Laser-Based Full Cut Dicing Evaluations for Thin Si wafers

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***Abstract*—Over the last years, singulation of thin semiconductor wafers with (ultra) low-K top layer has become a challenge in the production process of integrated circuits. The traditional blade dicing process is encountering serious yield issues. These issues can be addressed by applying a laser grooving process prior to the blade dicing, which is the process of reference nowadays. However, as wafers are becoming thinner, this process flow is not providing the yield and cost required. This paper will discuss the results of a study done on several multi beam laser ablation technologies on thin Si wafers and describe the pro's and con's for each of them.**

***Index Terms*—3D packaging, dicing, die strength, laser, thin wafer, multiple beams, diffractive optics**

I. INTRODUCTION

Full cut separation of semiconductor substrates has been the domain of a saw blade process for several decades [1]. Advances in the technology node, which require the use of low-K materials, have introduced laser technology in the IC wafer separation process [1]. The recent trend [2] to also reduce the substrate thickness drives the industry towards different separation technologies. We can distinguish two main areas which drive the substrate reduction [3]. The first one is the transition from 2-D to 3-D IC-packages that require thinner wafers (<50 um), which is already commonplace for memory and mobile applications. The second one is substrate thickness reduction to manage the heat dissipation and reduce internal resistance, which is typical for power devices such as IGBTs and MOSFETs.

The mechanical forces of the blade dicing process pose a serious challenge for thin wafer dicing [4, 5]. Wafers with low-K layers, that first require a laser grooving step [1], are even more challenging as the groove weakens the wafers resulting in a serious risk of wafer breakage. The semiconductor industry is still looking for a separation solution which provides high yield and productivity at low cost.

Section II starts by describing the method how die strength is measured. This is followed by Section III which describes the standard multi beam dicing process, benchmarked against the typical PoR's for thin wafer separation such as blade saw and Stealth dicing. An introduction and description of the processes developed for thin wafer dicing can be found in sections IV to VI. These processes are V-DOE, multi beam short pulse and nanosecond multi beam in combination with plasma etching. Each technology is reviewed for the die strength achieved and the overall dicing quality. Section VII compares the productivity for the different technologies. Finally, the overall comparison between the separation technologies and the conclusions are presented in section VIII.

II. DIE STRENGTH

All results mentioned in this paper have been measured on a 3 or 4-point die strength tool, both active structure up (SU) and structure down (SD) (see figure 1). The part of the sample that is facing down is subject to tensile stresses, which are generally responsible for the failure of the dies. To obtain good position accuracy of the support and loading edges while preventing friction effects, a measurement jig with an air bearing was employed.

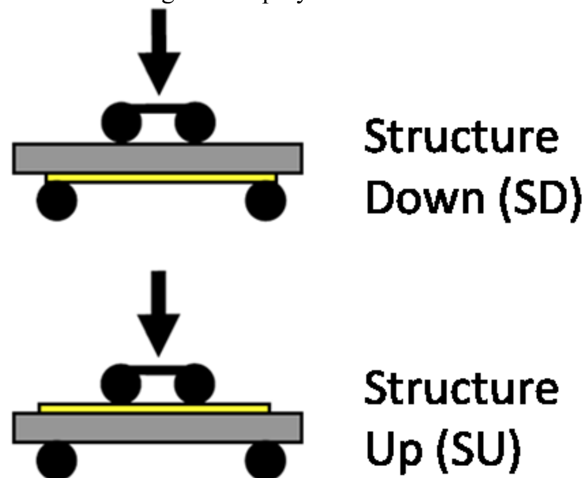

Figure 1. 4-point bending test for die strength measurements

III. MULTI BEAM LASER DICING

ASMPT's multi beam laser ablation dicing technology utilizes the patented multibeam technology. This technology has proven to achieve high yield and reliability, high productivity, a narrow kerf width, and a cost effective dicing solution at various assembly and packaging companies [6]. All of these criteria are advantages over the traditional separation technique; the blade dicing technique that is currently used in the industry. However, there is one criterion at which the standard multi beam dicing technology is not fulfilling the required specification which is the die strength.

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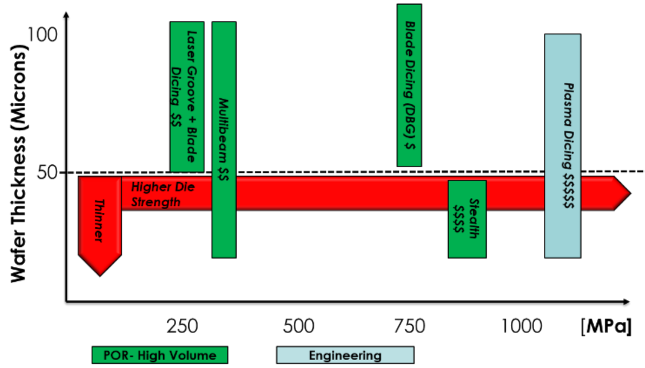

Figure 2. Die strength for various thin Si dicing technologies.

As shown in figure 2, the die strength of the multi beam dicing technology is on par with low-K grooving followed by blade dicing. But it is significantly lower compared to blade dicing or stealth dicing. In general, the target die strength value which a wafer dicing technology should achieve for thin Si wafers is 800 MPa or higher.

In the paper presented at ECTC in 2017 [7] we analyzed the root cause for the reduced die strength. It was found that during the rapid cooldown of the Si melt once the laser beams have passed by, various defects are formed. These defects range from voids and cracks in the micrometer range, to lattice defects in crystalline Si with otherwise the same orientation as the nearly defect-free monocrystalline substrate. When these defects are put under tension during die strength testing, we believe that they can cause early cracking of the die and therefore a reduction of the die strength.

To be able to address the issue of the reduced die strength, we investigated three different multi beam laser dicing technologies, each with their own characteristics.

IV. V-DOE LASER DICING

During studies performed last year [7] we found that by using low power laser beams along the edge of the dicing kerf, a laser annealing process can be established which partially removes the Heat Affected Zone (HAZ). Performing this type of laser annealing process with a single beam laser process requires a significant amount of time.

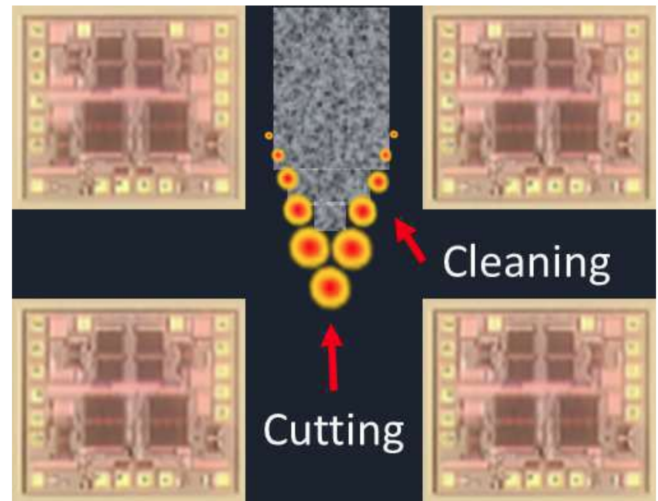

Figure 3. V-Shape spot pattern showing the central forward positioned spots which are used to dice through the wafer and the outer spots which clean the edges of the die.

Through using the multi beam technology a multi beam configuration, known as V-DOE, is established which allows both the dicing to take place as well as the cleaning/removal of the HAZ which the full cut process creates (see figure 3). When comparing the die strength results obtained from the multi beam and V-DOE processes on a 75-um thick polished Si wafer which was taped on a 20 um DAF tape a factor two improvement in the front side (structure down) die strength is found in favor of the V-DOE process. The die strength for the SU situation is already high due to the dicing parameters chosen for the dice through process. Therefore, the laser cleaning is only required on the top side of the die sidewall as is shown in figure 4.

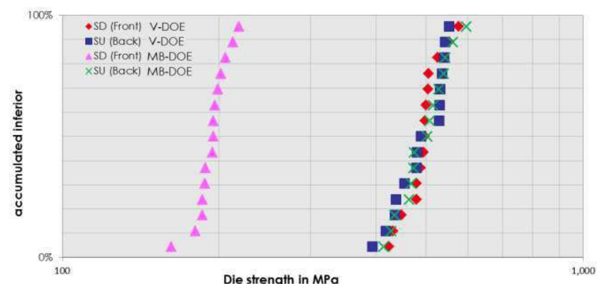

Figure 4. Die strength results SU & SD for standard multi beam (MB) laser dicing process and V-DOE process for a 75 um Si wafer on 20 um DAF measured on a 4-point bending tool.

Although this V-DOE process has shown a significant improvement in the die strength (factor 2x) and has been successfully qualified at several customers, it could not comply to the die strength established by PoR's such as saw blade or stealth dicing. This means that if customers maintain the adagio that a new wafer separation process should be able

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to meet the current die break strength level of a PoR, the process is not meeting this requirement.

V. SHORT PULSE DICING

As reported in several papers [8-11] short pulse lasers (femtosecond regime) are capable to dice wafer material with a minimized HAZ and therefore maintaining a good die strength. For many years, the laser power and pulse energy available from these lasers were insufficient to achieve the required throughput. In recent years, the power and pulse energy of short pulse lasers has significantly increased which motivated us to combine the multi beam dicing concept with these lasers. We performed a large range of dicing experiments in which we compared the die strength and dicing quality of a short pulse laser against more conventional nanosecond UV lasers.

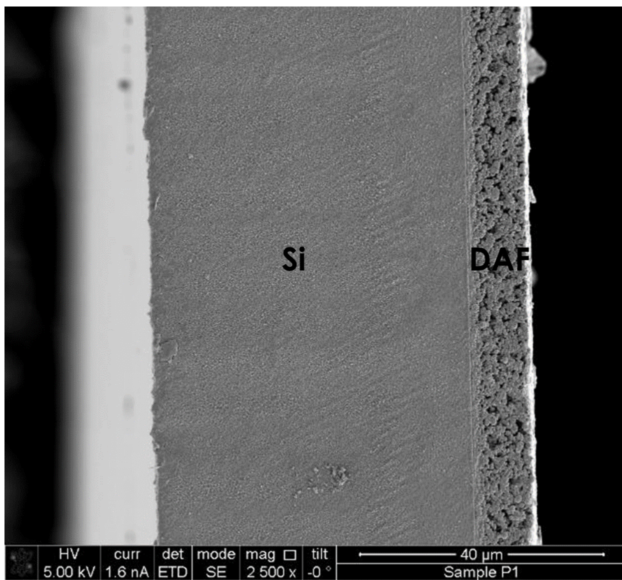

Figure 5. SEM micrograph of the sidewall dicing quality of a multi beam femtosecond process.

As shown in figure 5, the sidewall quality of the multi beam femtosecond laser shows a very smooth and well-controlled structure of both the Si and the Die Attach Foil (DAF).

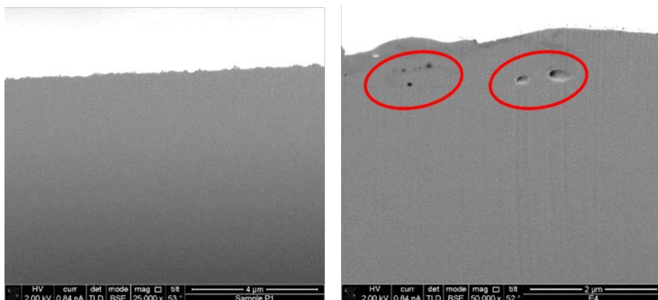

Figure 6. SEM micrographs of cross-sections of the sidewalls from femtosecond (left) and nanosecond (right) dicing processes.

Cross-section of sidewalls of laser-diced dies can be found in figure 6. No damage is visible by scanning electron microscopy for the femtosecond process while the nanosecond process shows voids. A reduction of the damage below the sidewall of the dies can result in an improved mechanical strength.

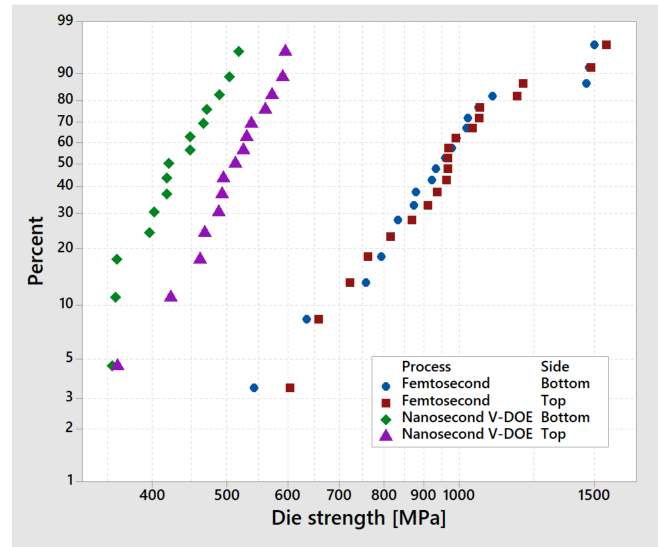

Figure 7. Comparison between the die strength (front side and backside) of nanosecond and femtosecond multi beam dicing.

Figure 7 demonstrates the die strength achieved on a 50 um polished Si wafer but the trend is similar for wafers with lithography active structures. Both the front side and backside die strength of the femtosecond dicing process are significantly improved compared to the nanosecond process.

VI. LASER AND PLASMA ETCHING

While the short pulse process is using cold ablation to prevent the formation of a HAZ and therefore maintains a good die strength, an alternative approach is to accept that it is created and remove it later on. ASMPT holds patents for this process [6] and for compound materials this process is applied in high volume production since 2006. For thin Si wafers, a similar process flow can be used in which the removal of the HAZ is done using a dry plasma etch. The main benefit of this process flow is that the strong point of the laser is used, the ability to dice through a stack of multiple layers (oxides, low-K, polymers, metal and Si), while the plasma etch process is used to etch away the 2-3 um wide HAZ which is created during the dicing process.

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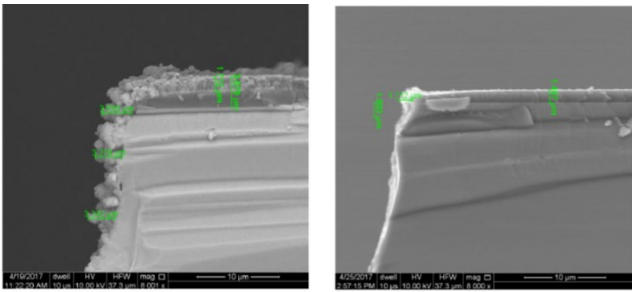

Figure 8. SEM micrographs of cross-sections of sidewalls before (left) and after plasma etching (right).

In figure 8, cross-sections are shown of the sidewall and top side of the die prior to and after the plasma etch process. As clearly shown, the plasma etch process removes the 2-3 um HAZ effectively and results in a HAZ-free sidewall. In the process flow, no photoresist is applied on the wafer prior to the plasma process. The standard polymer-based coating material used during the laser dicing step will also be used to protect the wafer surface during the etching process. The etching time will be shorter than the laser dicing allowing both process steps to take place in parallel without impacting the overall productivity of the laser dicing process.
The die strength recovery of this process outperforms any of the other dicing technologies reviewed in this paper as shown in figure 9.

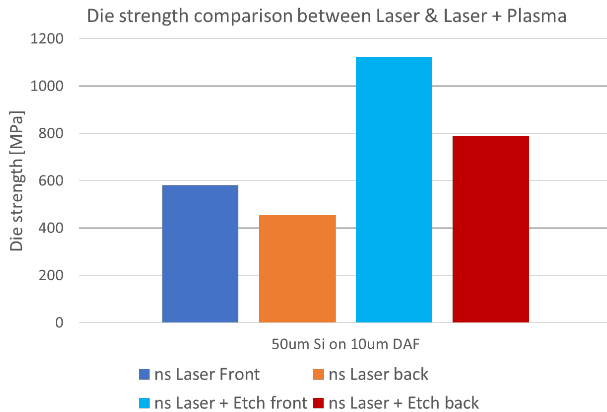

Figure 9. Die strength comparison between nanosecond laser dicing and nanosecond + plasma etch.

VII. PRODUCTIVITY

Apart from the fact that the wafer dicing technology has to meet the die strength and quality requirements, it also needs to be cost effective and therefore maintain a certain productivity.
Figure 10 provides an overview of the approximate productivity for the various dicing technologies reviewed.
A significant reduction in productivity can be observed for the femtosecond dicing process for larger wafer thicknesses (> 40 um). Further upscaling is required to obtain a competitive throughput for these wafer thicknesses. As the laser power development for short pulse lasers is increasing the plan is to combine ASMPT's patent for multi lane dicing with the multi beam dicing process. This allows to utilize the surplus of power and convert it into productivity.

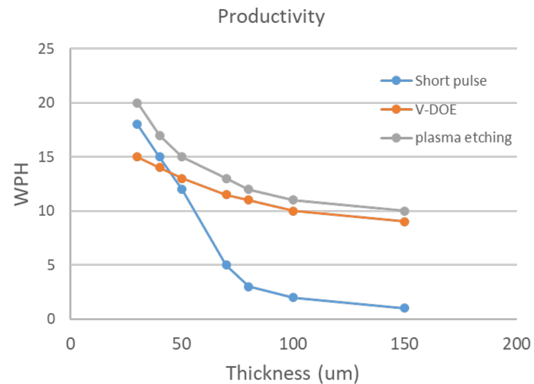

Figure 10. Productivity vs thickness for the various wafer separation technologies.

The benefit of the nanosecond process is that a significant part of the material removal process is through melt ejection, which is a more efficient way of removing material. Therefore, also for thicker substrates, a relatively high productivity can be achieved especially when comparing it to the short pulse femtosecond process.

VIII. CONCLUSIONS

All three different dicing technologies that were developed fill different market segments. As shown in figure 11, the V-DOE process achieves a die strength twice above the standard multi beam laser full cut dicing or laser grooving process. The V-DOE as reported [9] fulfills the qualification and reliability criteria and provides a high productivity with the minimum capex required. However, if the die strength achieved with this process does not meet the requirement of the product, two alternative dicing technologies can be used. First, the short pulse process which achieves a good die strength without the requirement of a post-process step. However the wafer thickness regime in which it can currently be applied is limited to approx. 40 um. For memory wafers, the volume is already below 40 um wafer thickness. Having a dicing technology which can cover this and be able to dice the increased active layer thickness (specifically for 3D NAND) while maintaining sufficient die strength, gives it a strong potential. However, if the application requires thicker wafers than 40 um which also have a multi-layer stack of materials, the nanosecond laser dicing process in combination with plasma etching provides a good productivity and die strength. This process flow does require additional capex however this will be significantly lower (factor 5 to 6) compared to the plasma dicing systems available in the market which can only dice Si.

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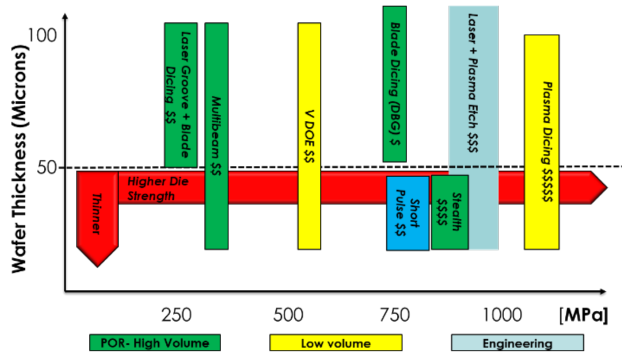

Figure 11. Die strength for various Thin Si dicing technologies including V-DOE, short pulse and laser plus plasma etch.

We therefore believe that with the three wafer separation technologies, a broad spectrum of the thin wafer dicing market can be served.

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