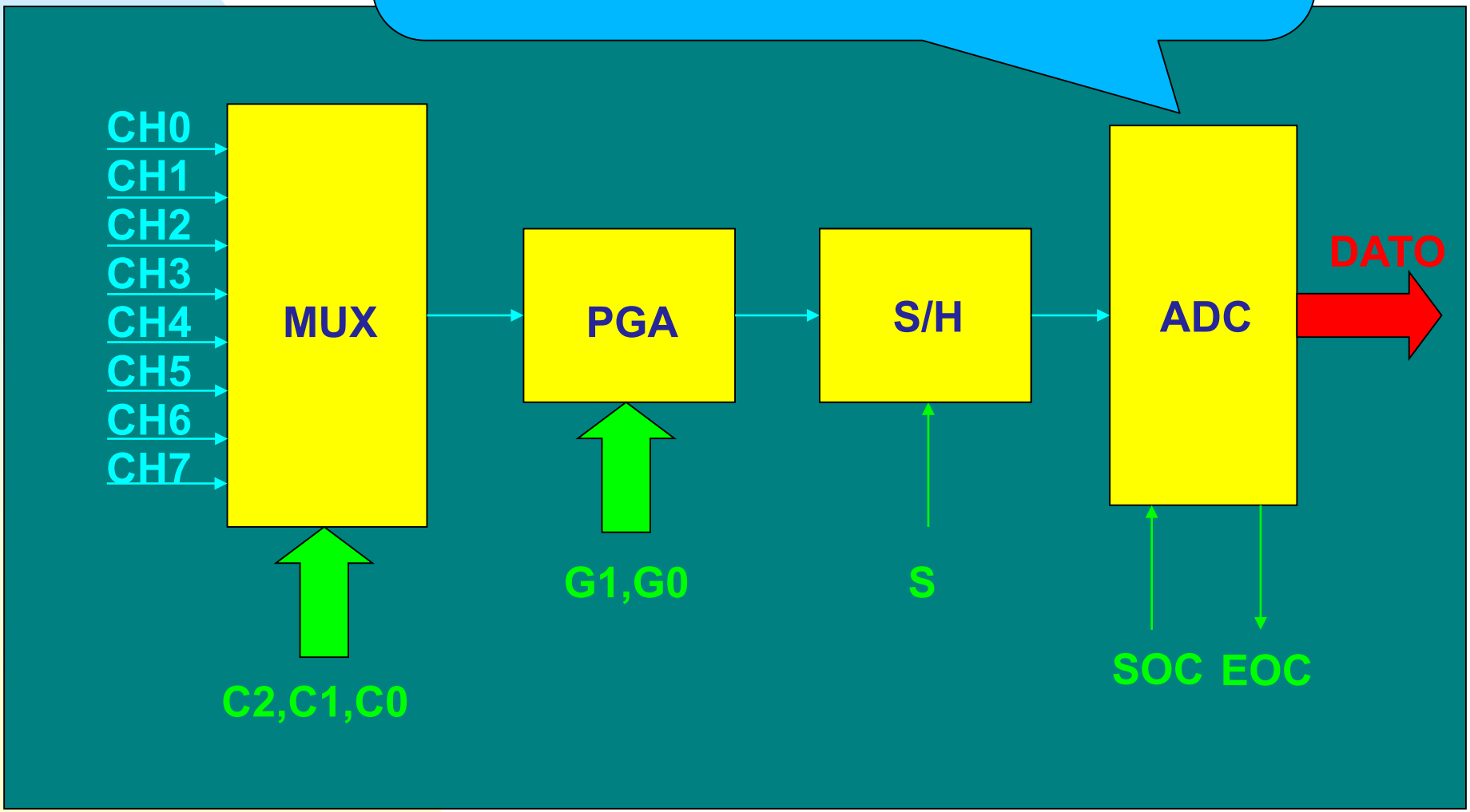
Analog/Digital Converters

Luis Zorzano Martínez

Analog/Digital Converters



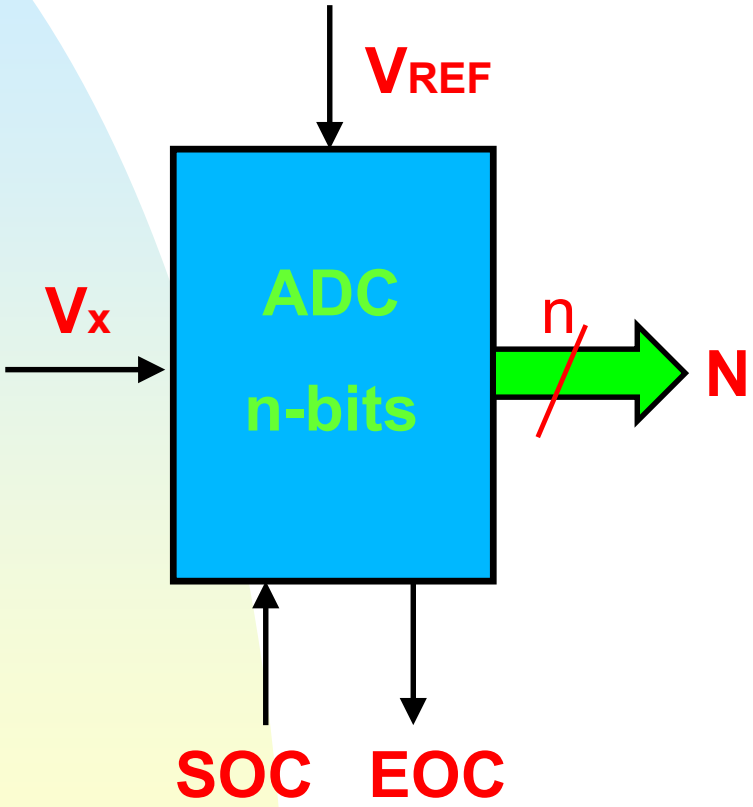
Analog/Digital Converters

Definición

Tipos de ADCs

Aplicaciones

Analog/Digital Converters



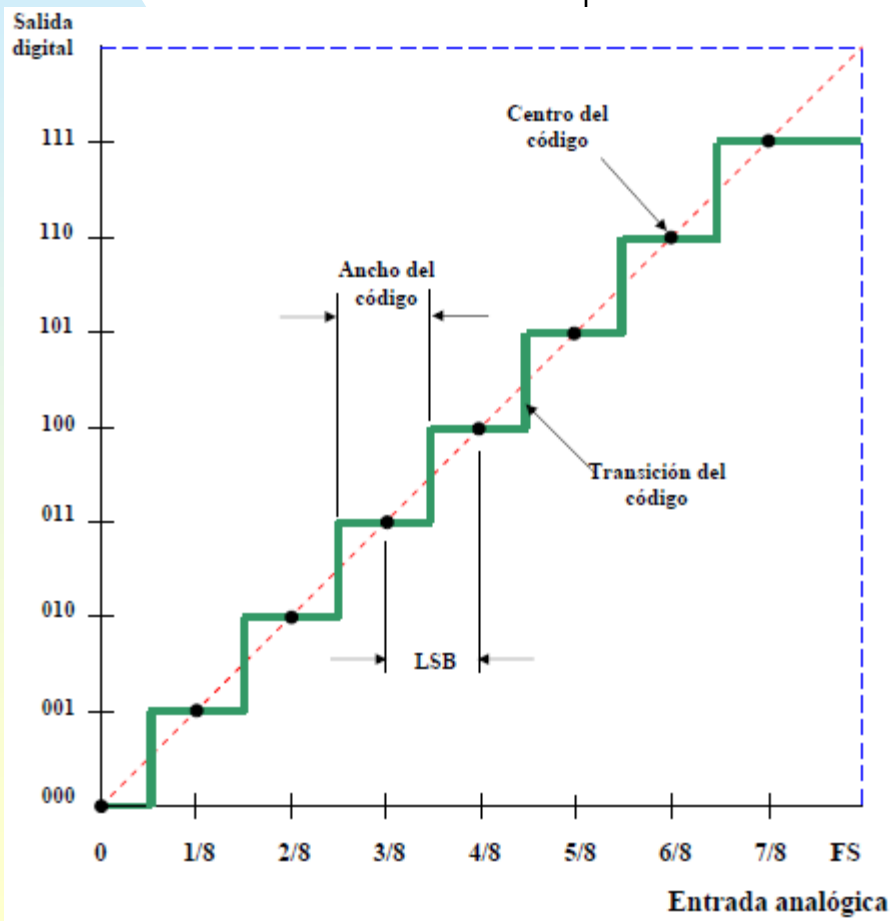
ADC unipolar

$$N = round\left(\frac{V_x}{V_{REF}} 2^n\right)$$

ADC bipolar

$$N = round\left(\frac{V_X - \left(-V_{REF}\right)}{2V_{REF}} 2^n\right)$$

Analog/Digital Converters



CÓDIGOS UNIPOLARES

- CÓDIGO BINARIO NATURAL
- CÓDIGO BINARIO INVERTIDO
- CÓDIGO BCD
- CODIGO GRAY

$$N = round\left(\frac{V_x}{V_{REF}}2^n\right)$$

CÓDIGOS BIPOLARES

- CÓDIGO BINARIO DECALADO
- CÓDIGO COMPLEMENTO A 2
- CÓDIGO COMPLEMENTO A 1
- CÓDIGO BINARIO+SIGNO

$$N = round\left(\frac{V_X - \left(-V_{REF}\right)}{2V_{REF}}2^n\right)$$

ADC: Códigos Unipolares

N	BN	BI	BCD	GRAY
15	1111	0000	1 0101	1000
14	1110	0001	1 0100	1001
13	1101	0010	1 0011	1011
12	1100	0011	1 0010	1010
11	1011	0100	1 0001	1110
10	1010	0101	1 0000	1111
9	1001	0110	0 1001	1101
8	1000	0111	0 1000	1100
7	0111	1000	0 0111	0100
6	0110	1001	0 0110	0101
5	0101	1010	0 0101	0111
4	0100	1011	0 0100	0110
3	0011	1100	0 0011	0010
2	0010	1101	0 0010	0011
1	0001	1110	0 0001	0001
0	0000	1111	0 0000	0000

CÓDIGOS UNIPOLARES

- CÓDIGO BINARIO NATURAL
- CÓDIGO BINARIO INVERTIDO
- CÓDIGO BCD
- CODIGO GRAY

$$N = round\left(\frac{V_x}{V_{REF}} 2^n\right)$$

ADC: Códigos Bipolares

N	B+S	BO	CA2	CA1
7	1111	1111	0111	0111
6	1110	1110	0110	0110
5	1101	1101	0101	0101
4	1100	1100	0100	0100
3	1011	1011	0011	0011
2	1010	1010	0010	0010
1	1001	1001	0001	0001
0	1000	1000	0000	0000
-0	0000			1111
-1	0001	0111	1111	1110
-2	0010	0110	1110	1101
-3	0011	0101	1101	1100
-4	0100	0100	1100	1011
-5	0101	0011	1011	1010
-6	0110	0010	1010	1001
-7	0111	0001	1001	1000
-8		0000	1000	

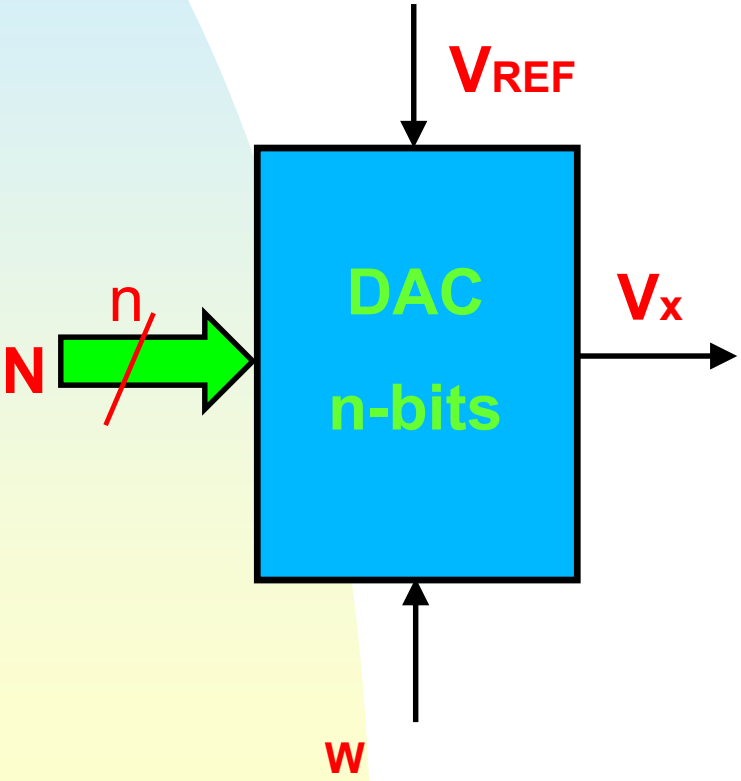
CÓDIGOS BIPOLARES

- CÓDIGO BINARIO DECALADO (B.O.)
- CÓDIGO COMPLEMENTO A 2
- CÓDIGO COMPLEMENTO A 1
- CÓDIGO BINARIO+SIGNO

$$N = round\left(\frac{V_X - \left(-V_{REF}\right)}{2V_{REF}} 2^n\right)$$

DAC: antes de los ADCs

- Muchos ADCs incorporan DACs
- DAC: Digital Analog Converter

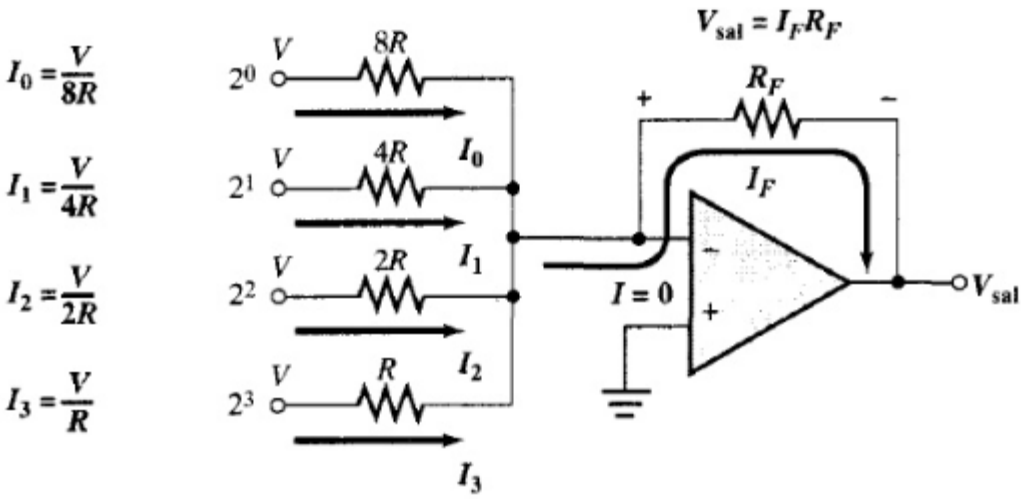


DAC

$$V_x = \left(\frac{N}{2^n} V_{REF} \right)$$

DAC con resistencias ponderadas

Convertidor Analógico Digital de 4 bits con resistencias ponderadas



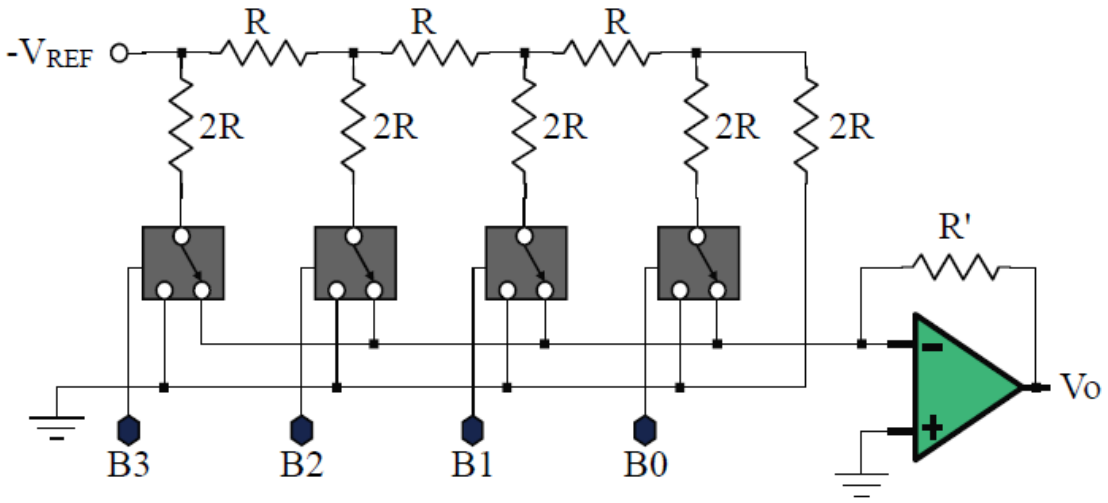
Un convertidor D/A de 4 bits (DAC) con entradas ponderadas en binario.

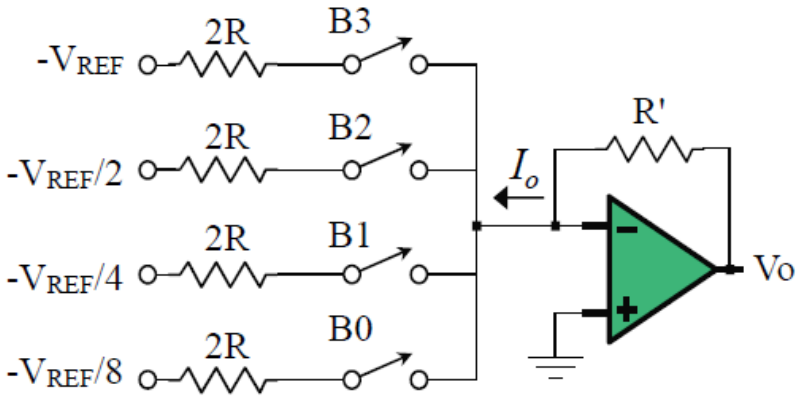
$$V_{sal} = -R_F I_F = -R_F \sum_{i=0}^{3} b_i I_i = -R_F \sum_{i=0}^{3} b_i \frac{V}{R_i} = -R_F \sum_{i=0}^{3} b_i \frac{V}{2^{3-i}R} =$$

$$V_{sal} = -V \frac{R_F}{2^3 R} \sum_{i=0}^{3} b_i 2^i = -V \frac{R_F}{2^3 R} N$$

DAC en escalera R/2R

DAC en escalera R/2R

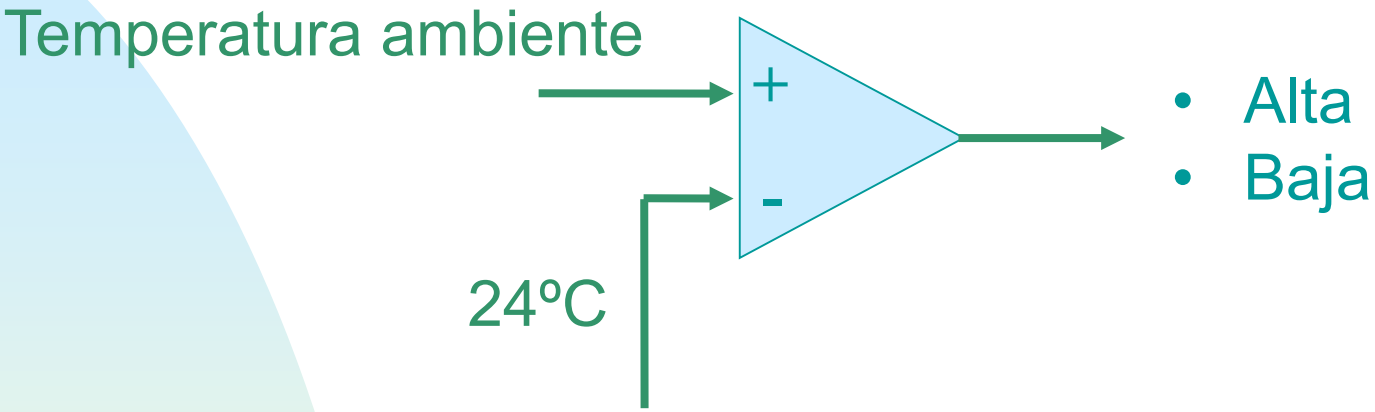




$$I_o = \frac{V_{ref}}{2^n R} \cdot \sum_{i=0}^{n-1} 2^i \cdot Bi$$

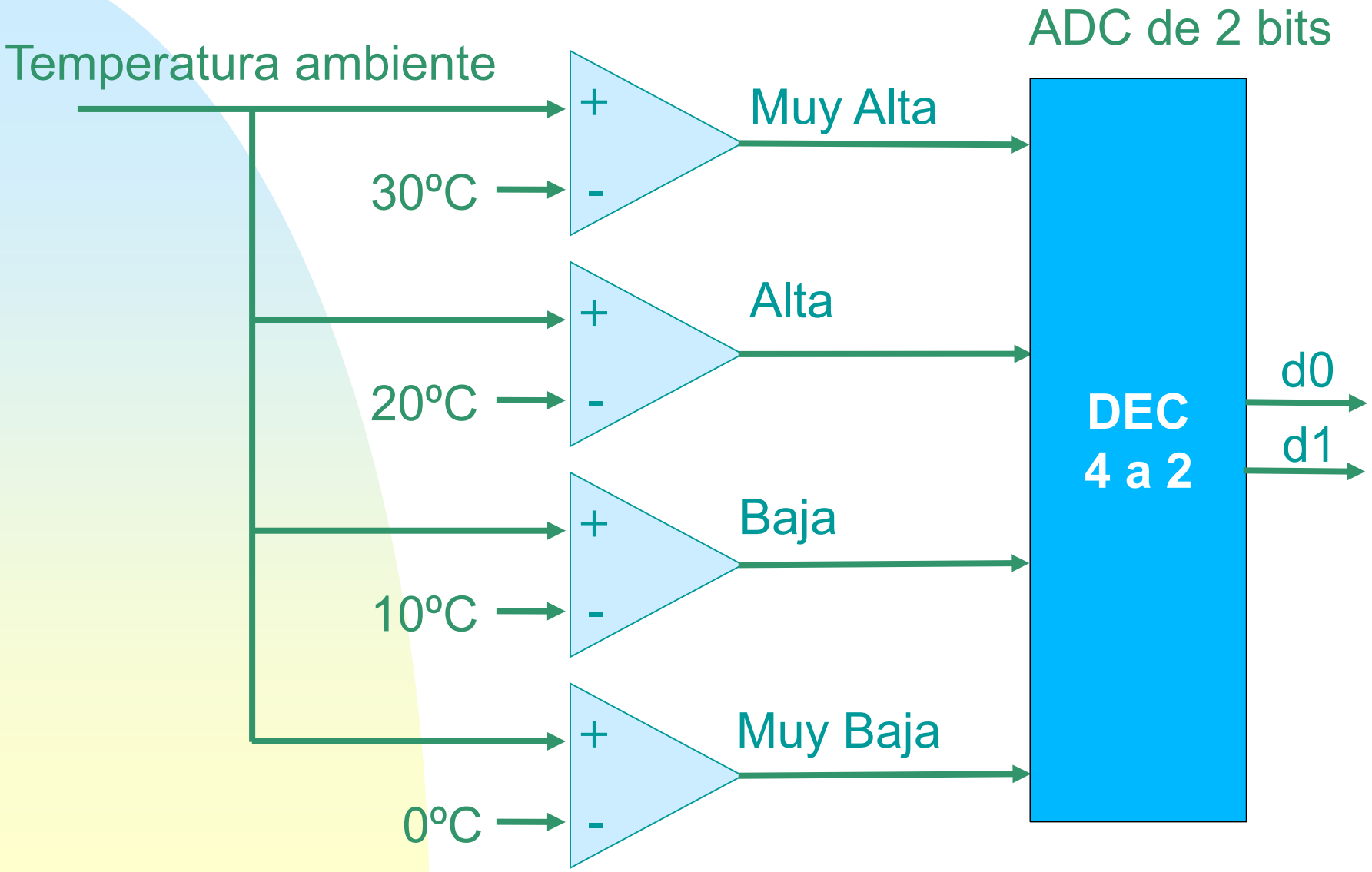
$$V_o = \frac{V_{ref}}{2^n} \cdot \sum_{i=0}^{n-1} 2^i \cdot Bi$$

ADC: Principio básico

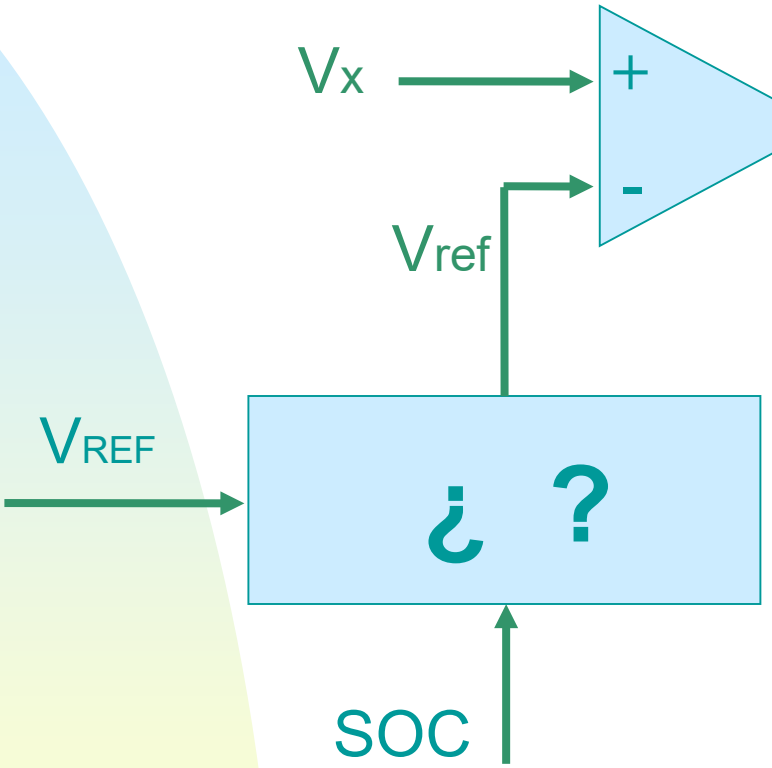


ADC de 1 bit

ADC: Principio básico



ADC: Principio básico

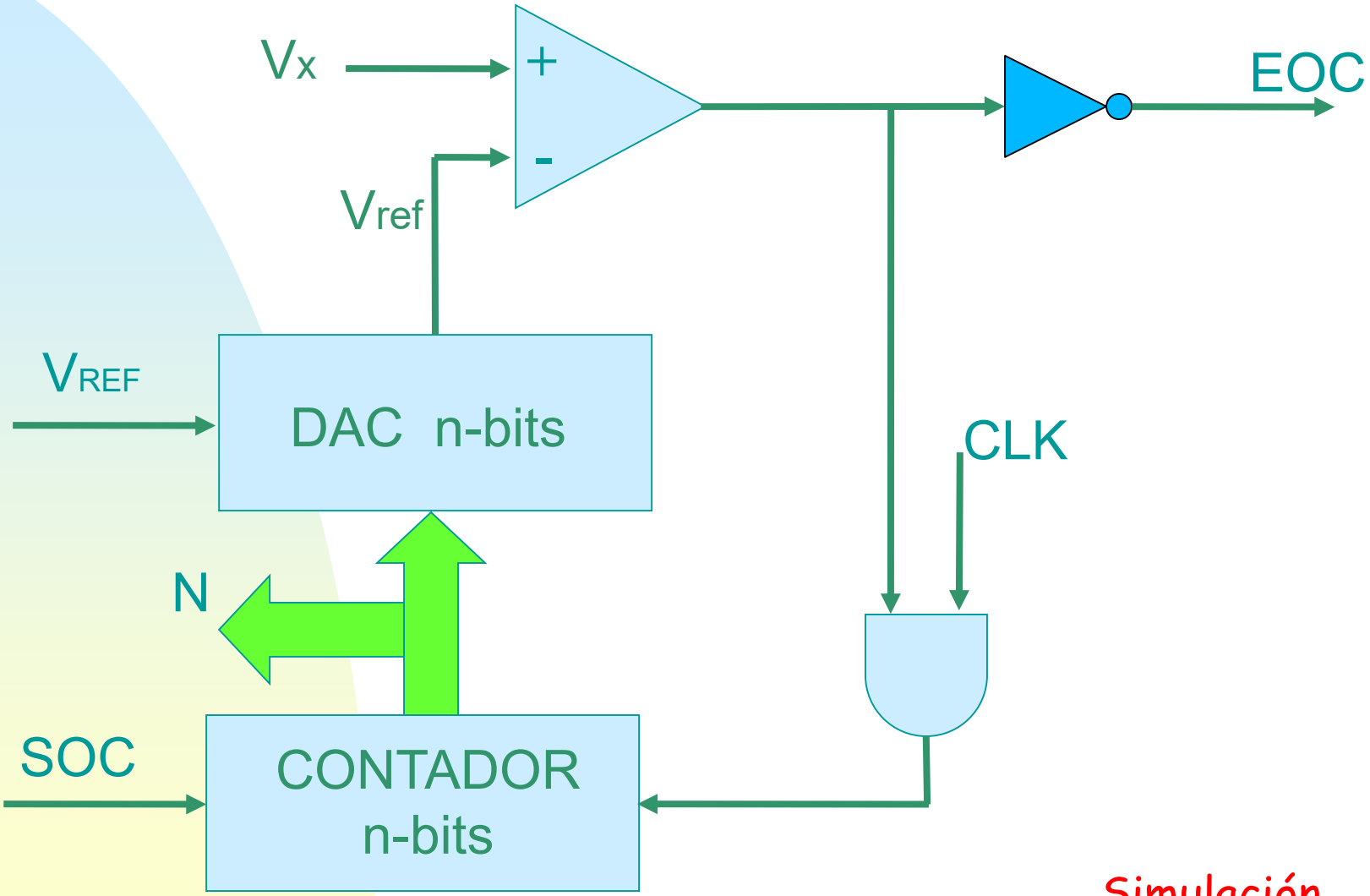


- ADC rampa contador
- ADC servoconversor
- ADC SAR
- ADC rampa
- ADC doble rampa
- ADC Flash
- ADC Half-Flash
- ADC Sigma-Delta

Tipos de convertidores

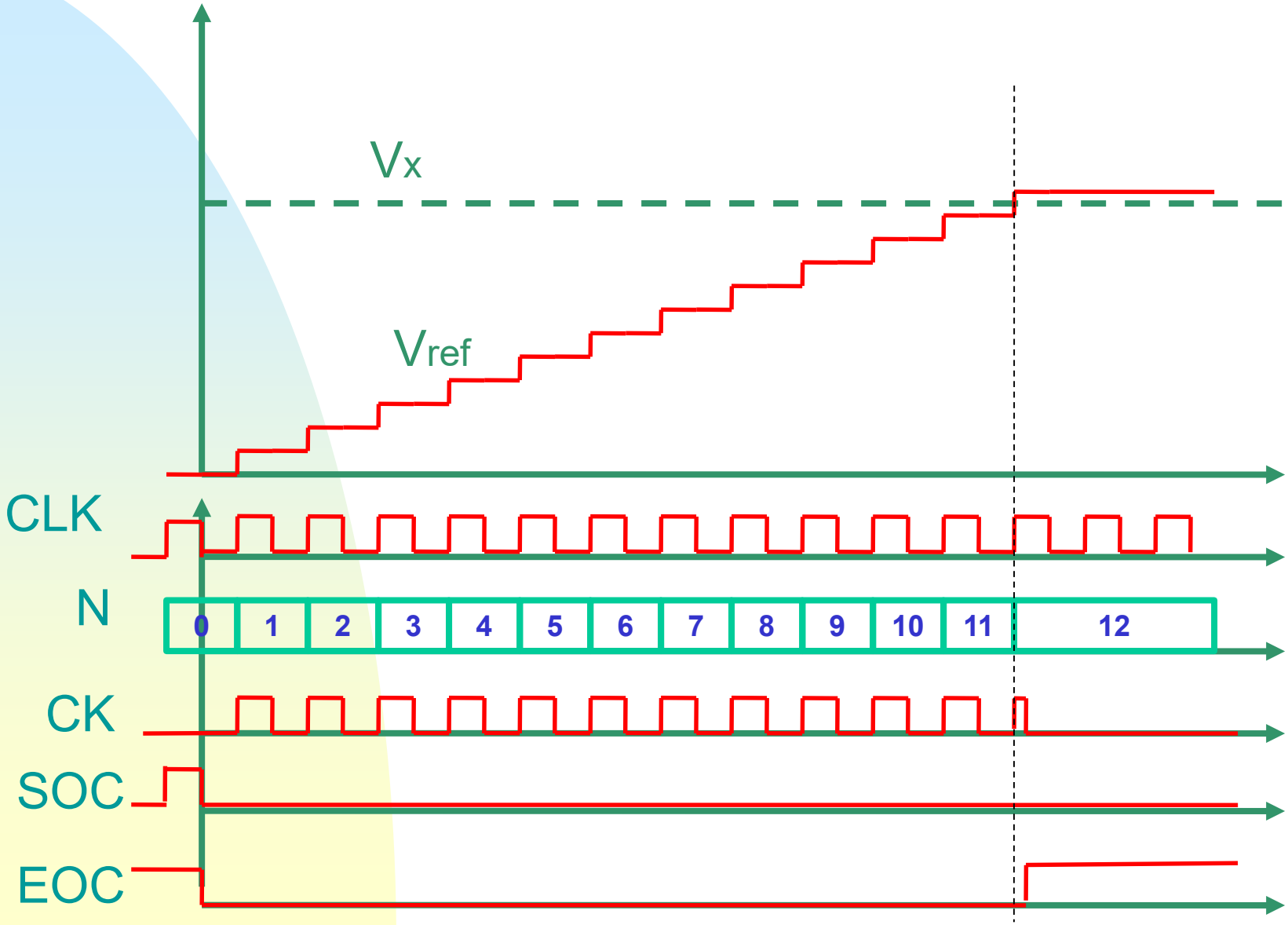
- ADC rampa contador
- ADC servoconversor
- ADC SAR
- ADC rampa
- ADC doble rampa
- ADC Flash
- ADC Half-Flash
- ADC Sigma-Delta

ADC rampa-contador

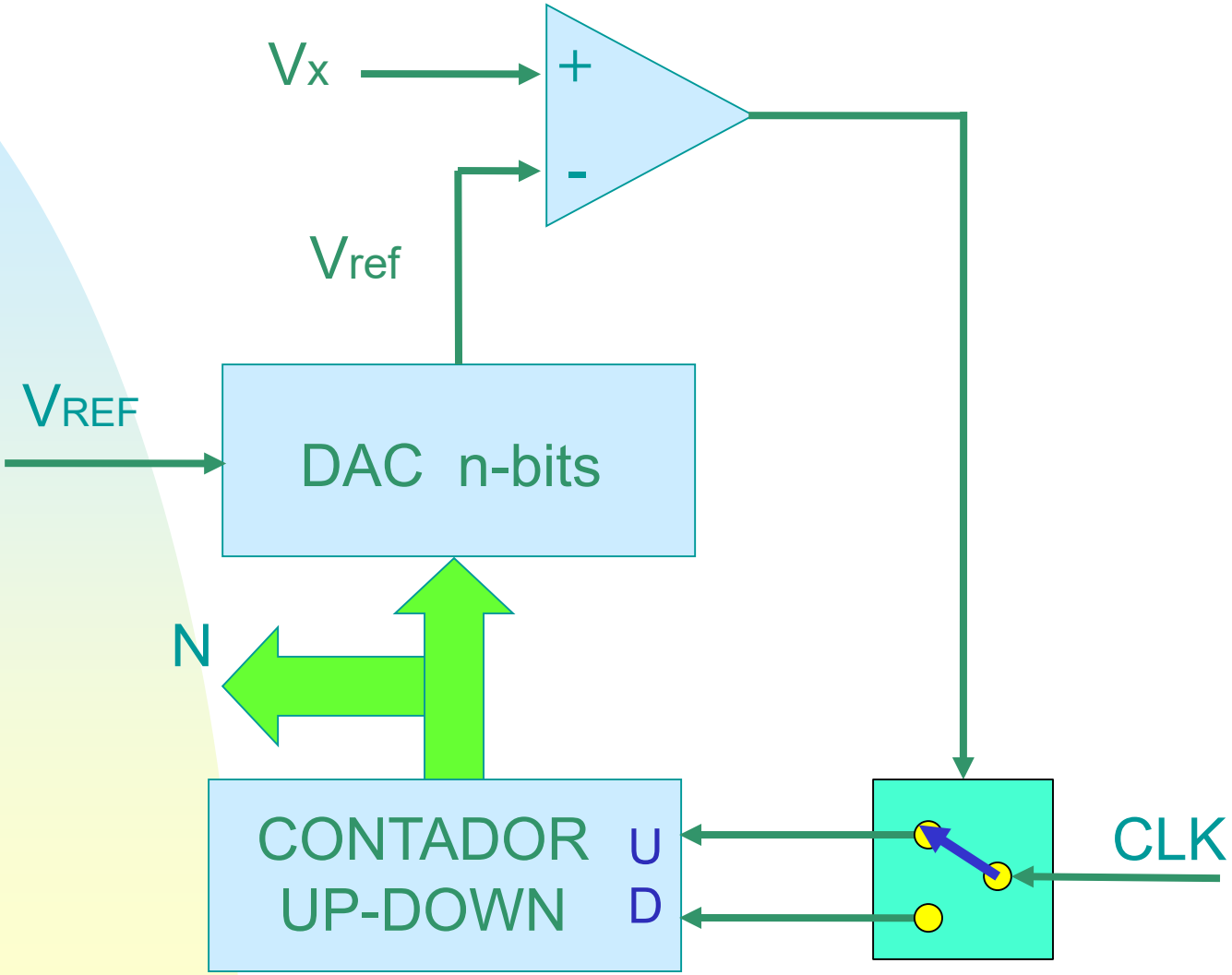


Simulación

ADC rampa-contador

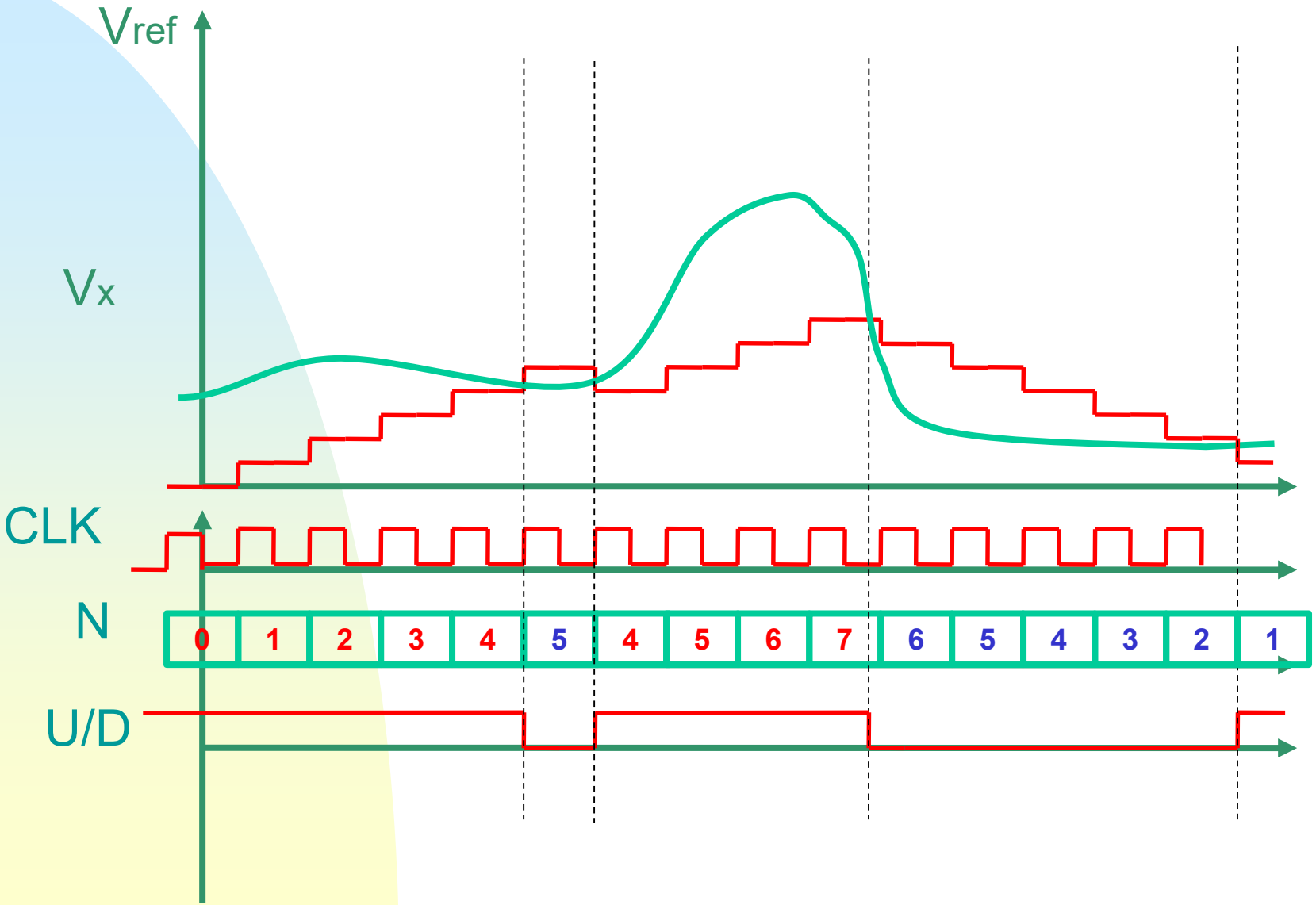


ADC servoconversor

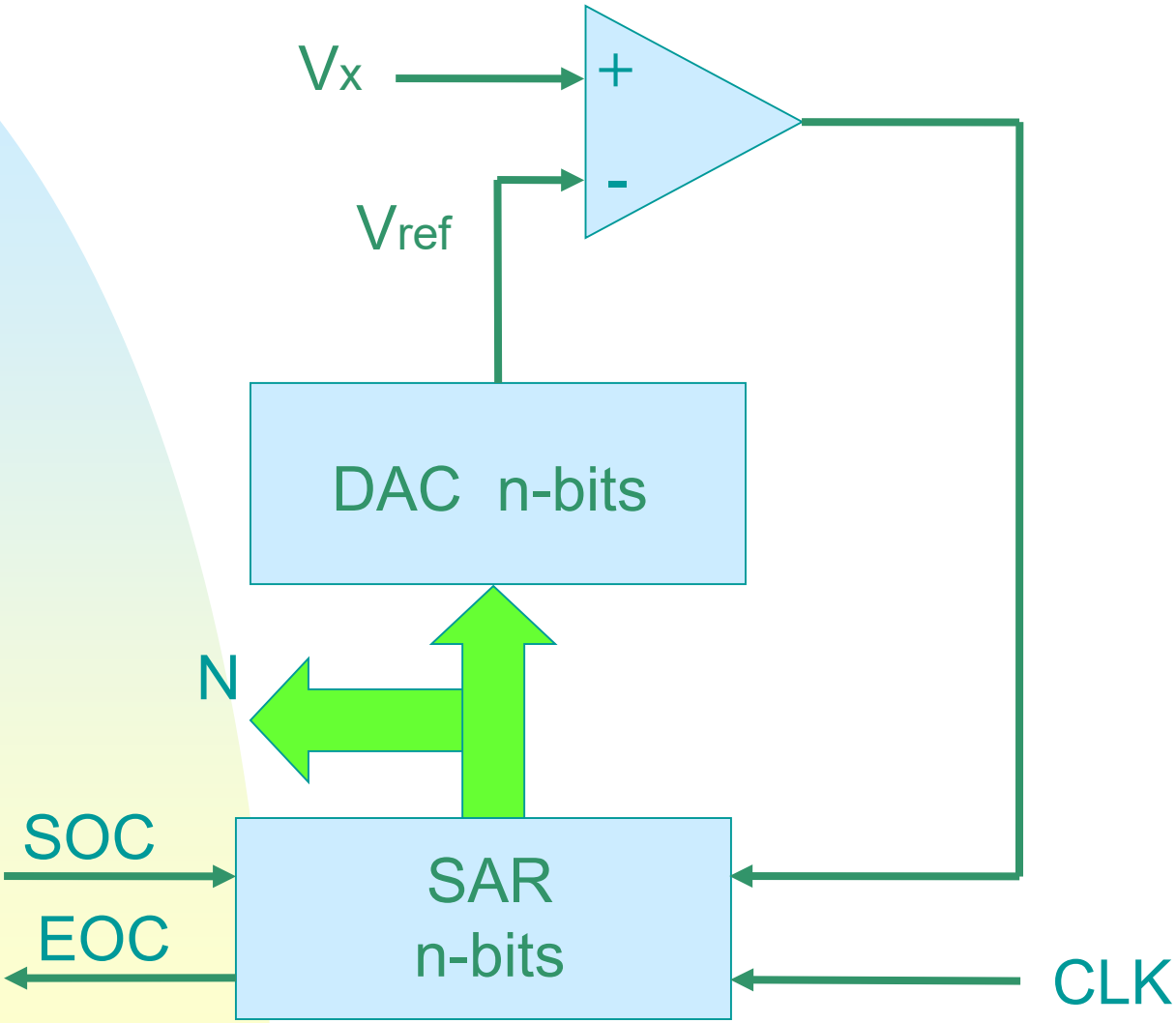


Simulación

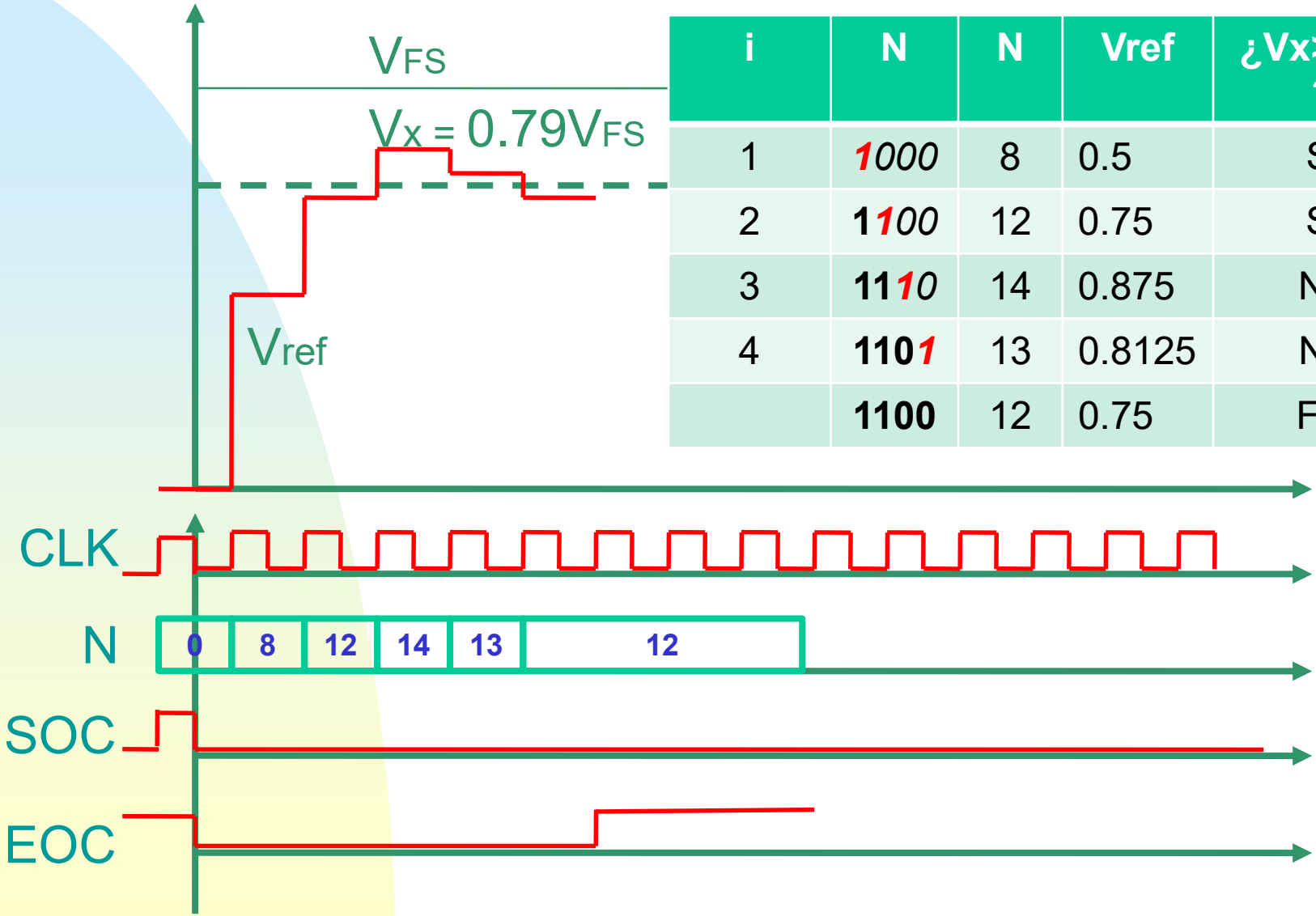
ADC servoconversor



ADC SAR

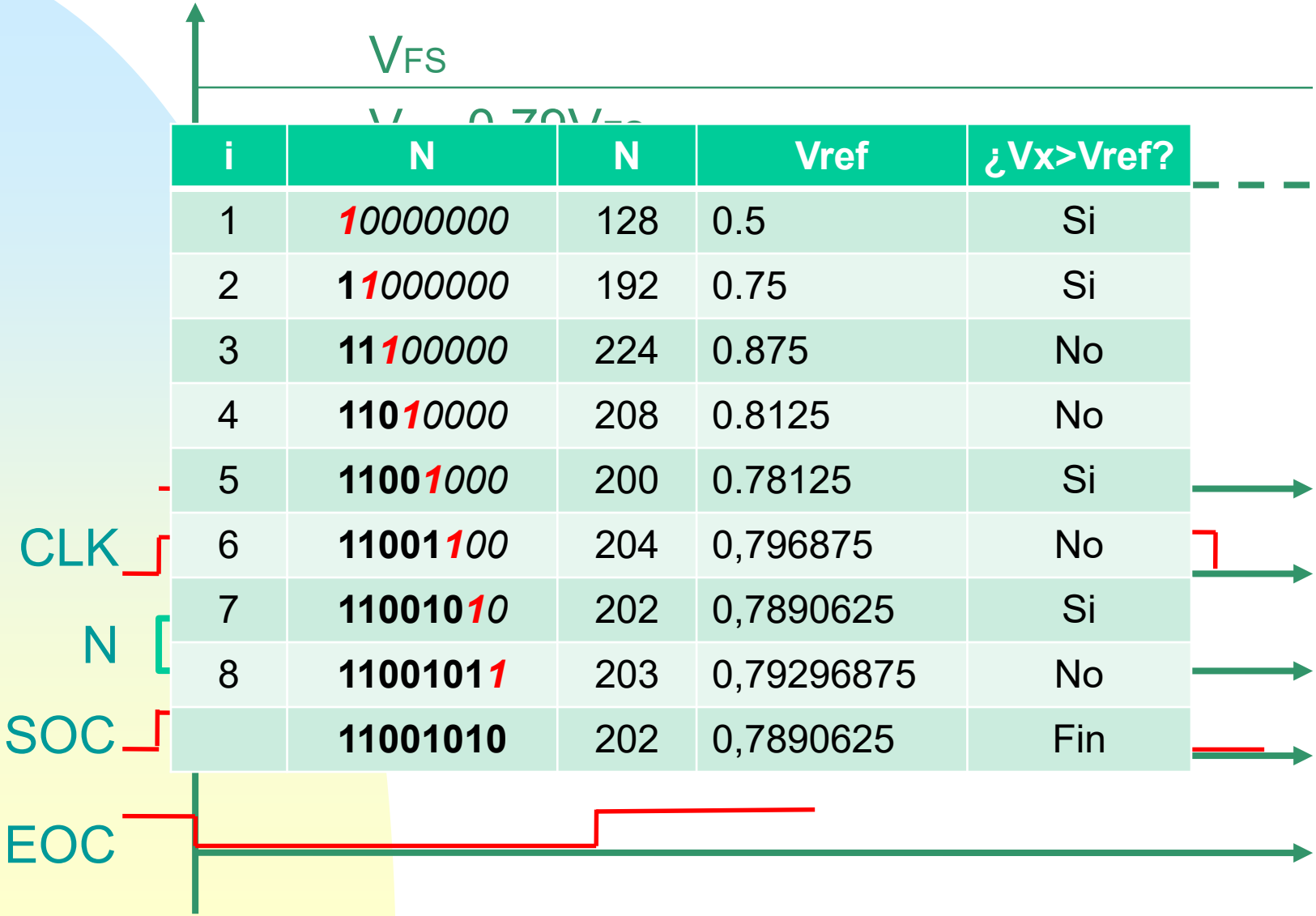


ADC SAR



i	N	N	Vref	¿Vx>Vref ?
1	*1*000	8	0.5	Si
2	1*1*00	12	0.75	Si
3	11*1*0	14	0.875	No
4	110*1*	13	0.8125	No
	1100	12	0.75	Fin

ADC SAR 8 bits



i	N	N	Vref	¿Vx>Vref?
1	***1***0000000	128	0.5	Si
2	**1*1***000000	192	0.75	Si
3	**11*1***00000	224	0.875	No
4	**110*1***0000	208	0.8125	No
5	**1100*1***000	200	0.78125	Si
6	**11001*1***00	204	0,796875	No
7	**110010*1*0	202	0,7890625	Si
8	**1100101*1*	203	0,79296875	No
	11001010	202	0,7890625	Fin

ADC SAR sc

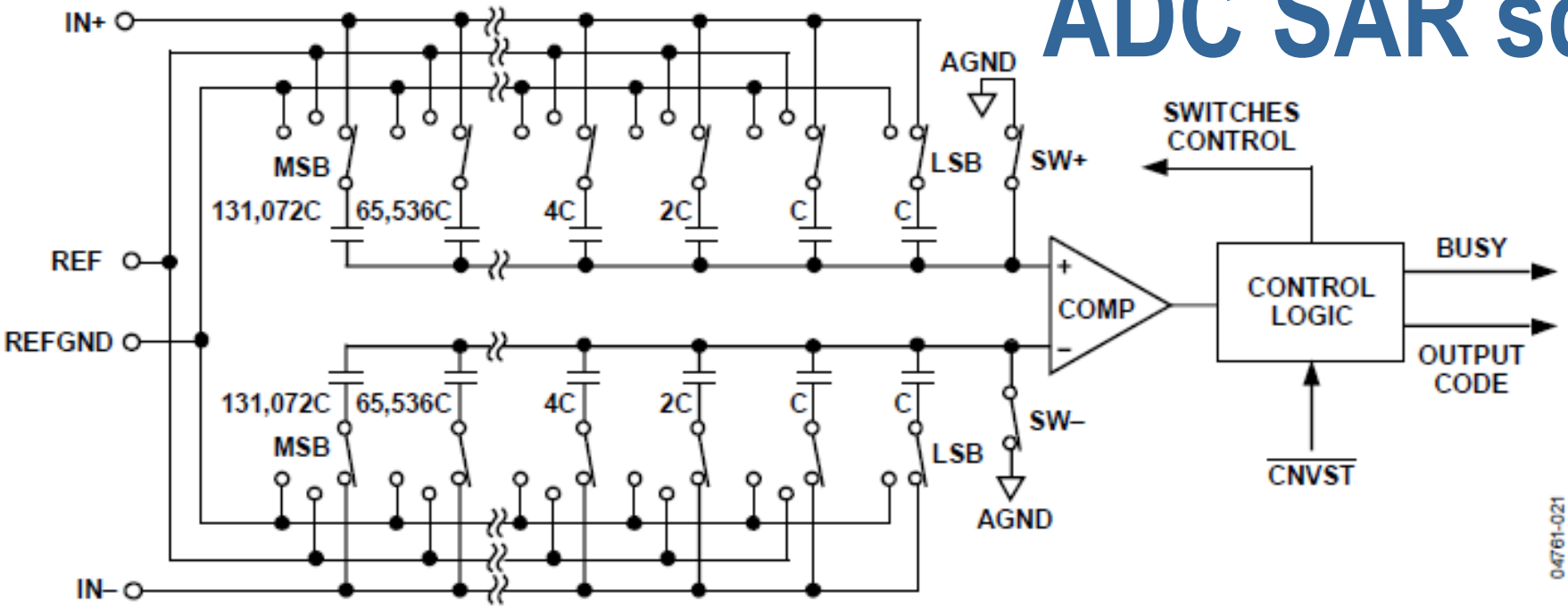
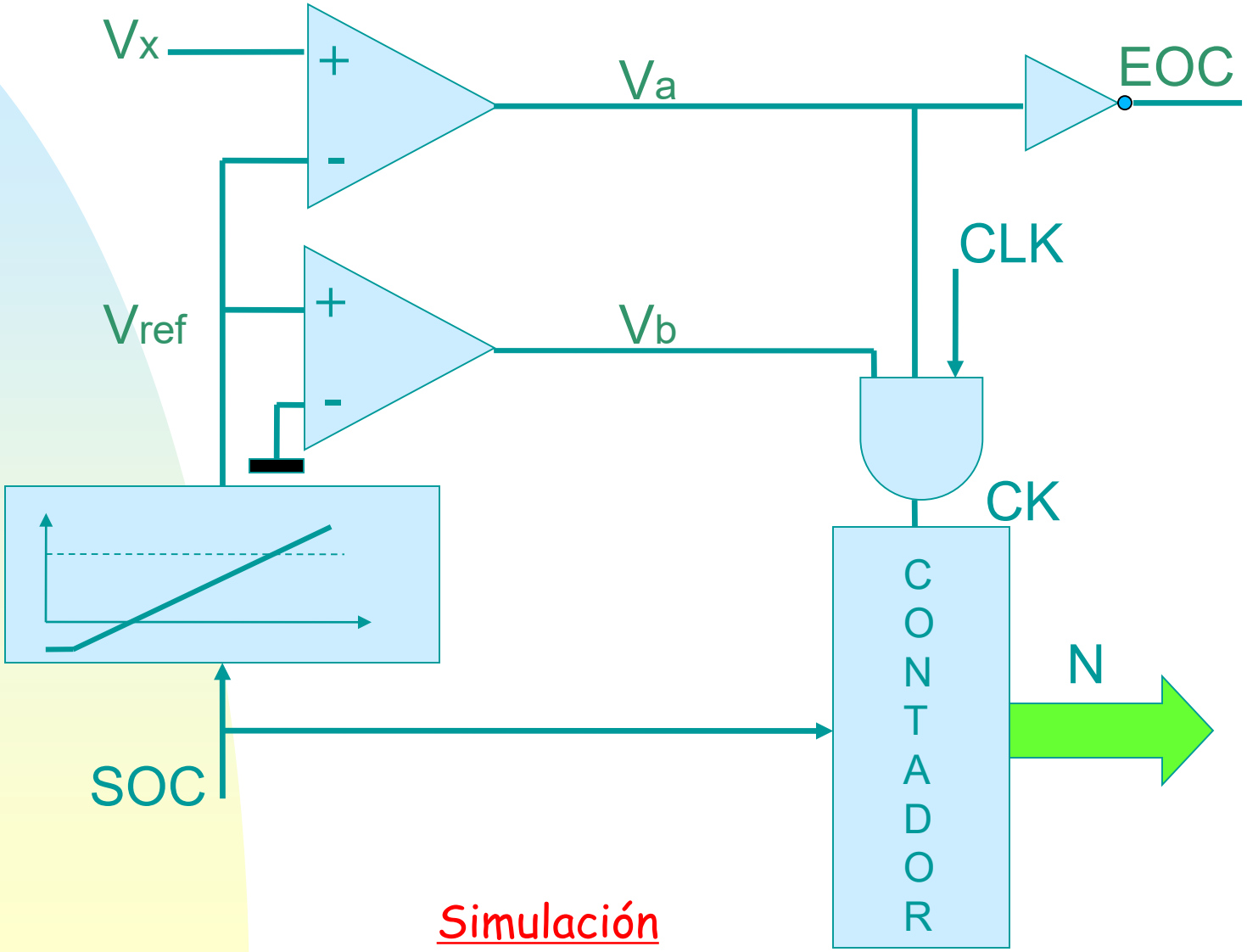


Figure 21. ADC Simplified Schematic

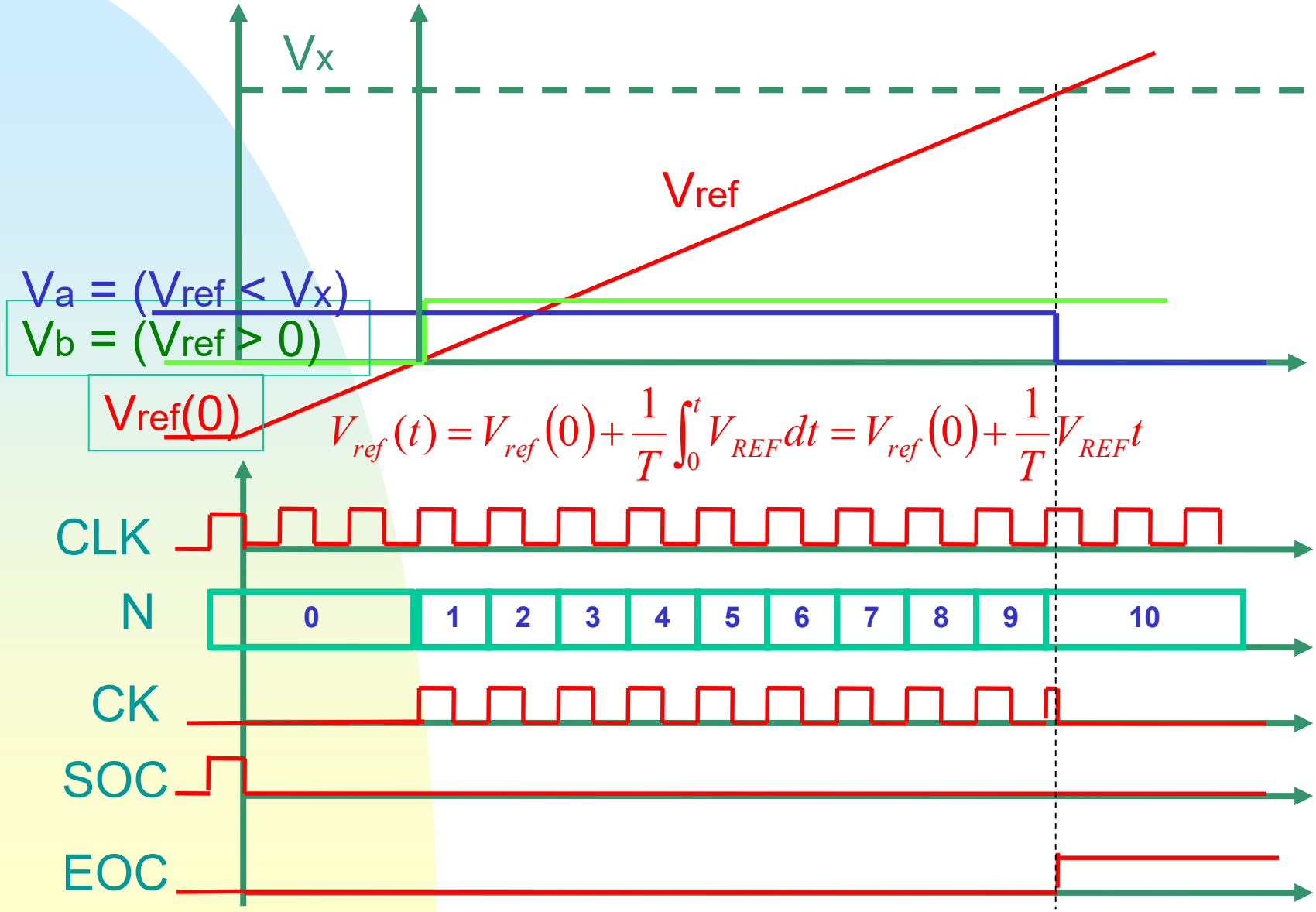
During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW–. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN– inputs. A conversion phase is initiated once the acquisition phase is complete and the CNVST input goes low. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN–) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/131072$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

ADC simple rampa

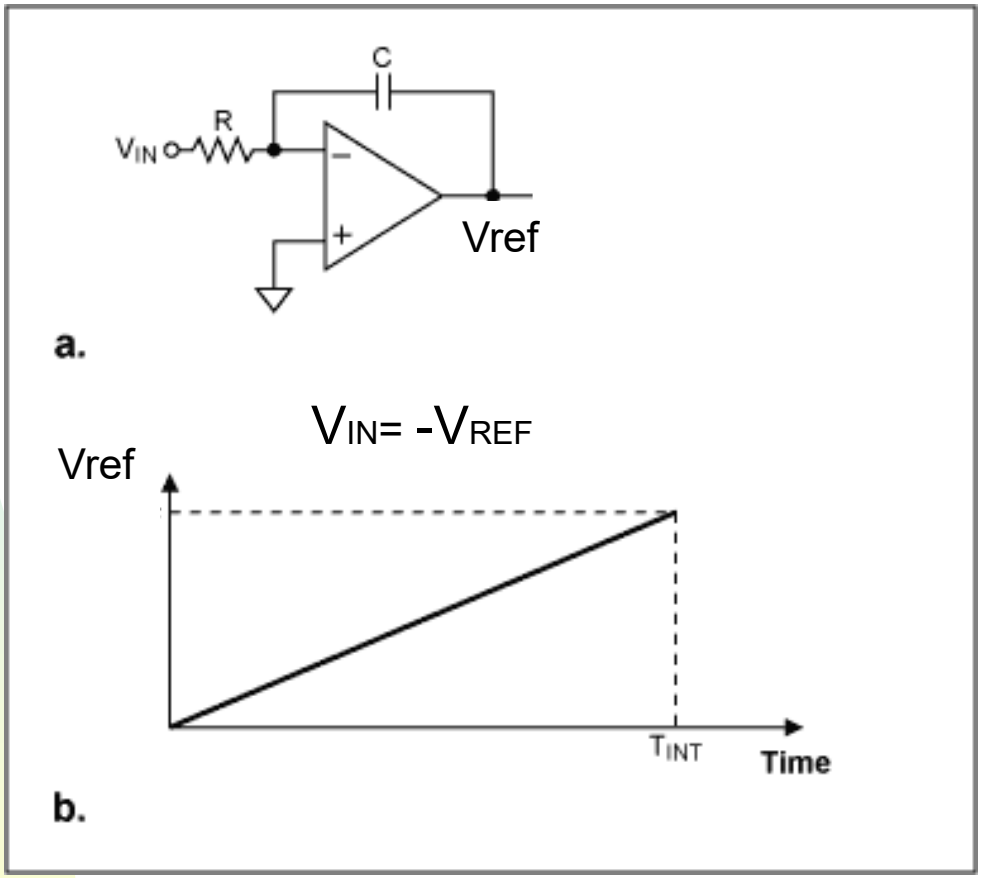


Simulación

ADC simple rampa

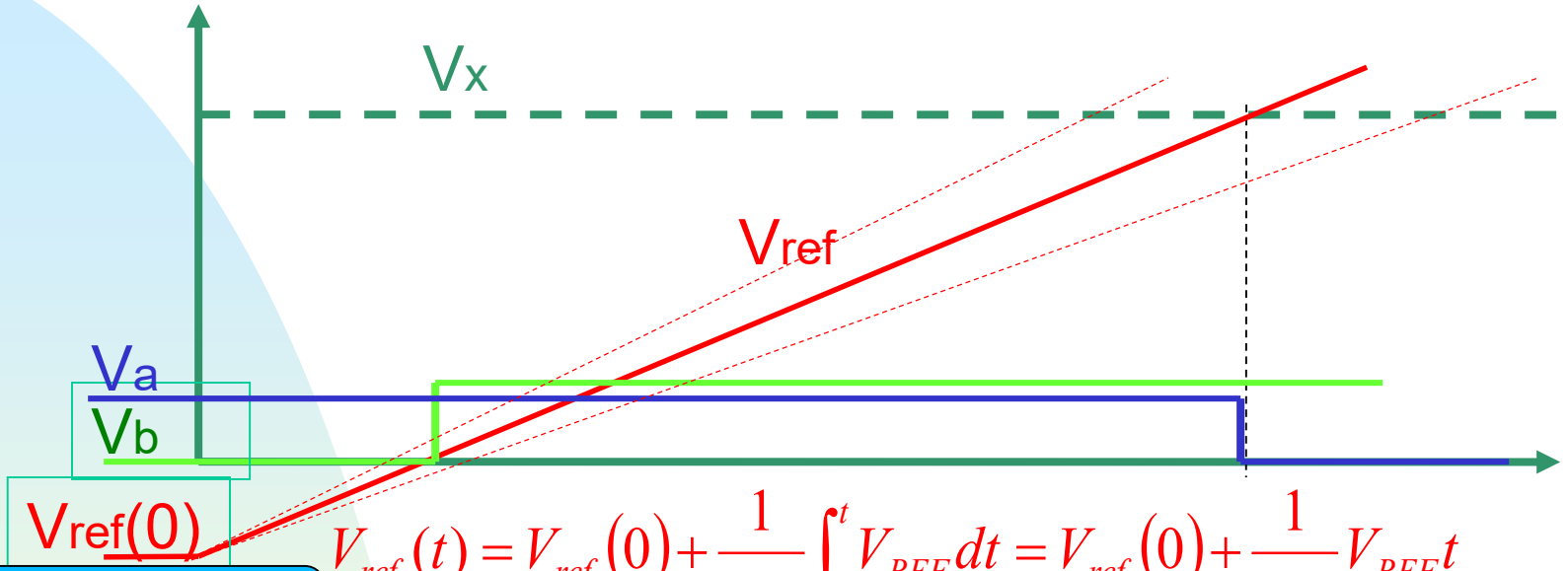


ADC simple rampa



$$V_{ref}(t) = V_{ref}(0) - \frac{1}{RC}\int_0^t V_{IN}\,dt = V_{ref}(0) + \frac{1}{RC}\int_0^t V_{REF}\,dt = V_{ref}(0) + \frac{1}{RC}V_{REF}t$$

ADC simple rampa



$$V_{ref}(t) = V_{ref}(0) + \frac{1}{RC}\int_0^t V_{REF}\,dt = V_{ref}(0) + \frac{1}{RC}V_{REF}t$$

Ecuación definida en el tiempo de ejecución

$$V_x = V_{ref}(t = N \cdot T_{CK}) = \frac{1}{RC}V_{REF} \cdot N \cdot T_{CK}$$

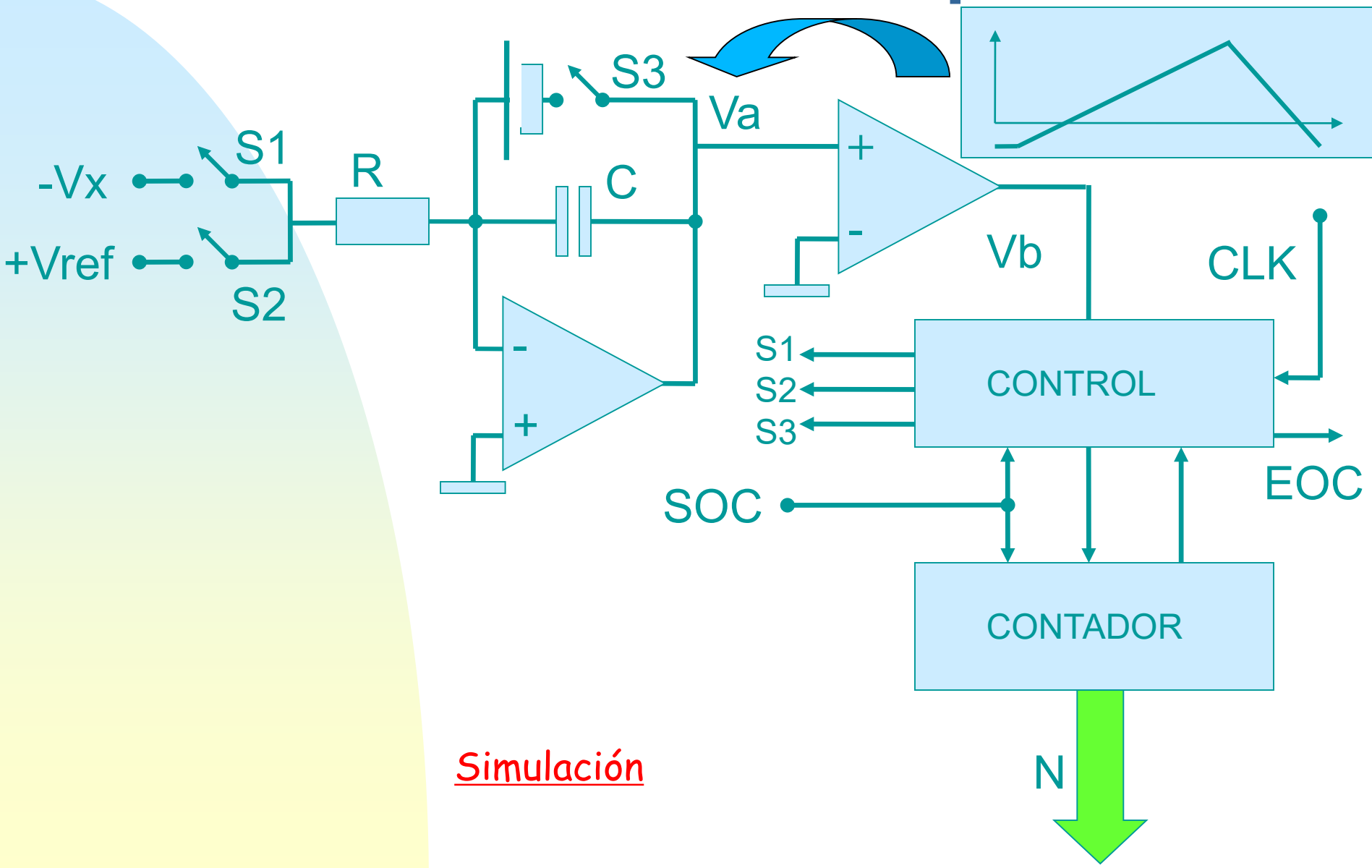
$$V_{FS} = V_{ref}(t = 2^n \cdot T_{CK}) = \frac{1}{RC}V_{REF} \cdot 2^n \cdot T_{CK}$$

$$\frac{V_x}{V_{FS}} = \frac{\frac{1}{RC}V_{REF} \cdot N \cdot T_{CK}}{\frac{1}{RC}V_{REF} \cdot 2^n \cdot T_{CK}}$$

Ecuación definida en el tiempo de diseño

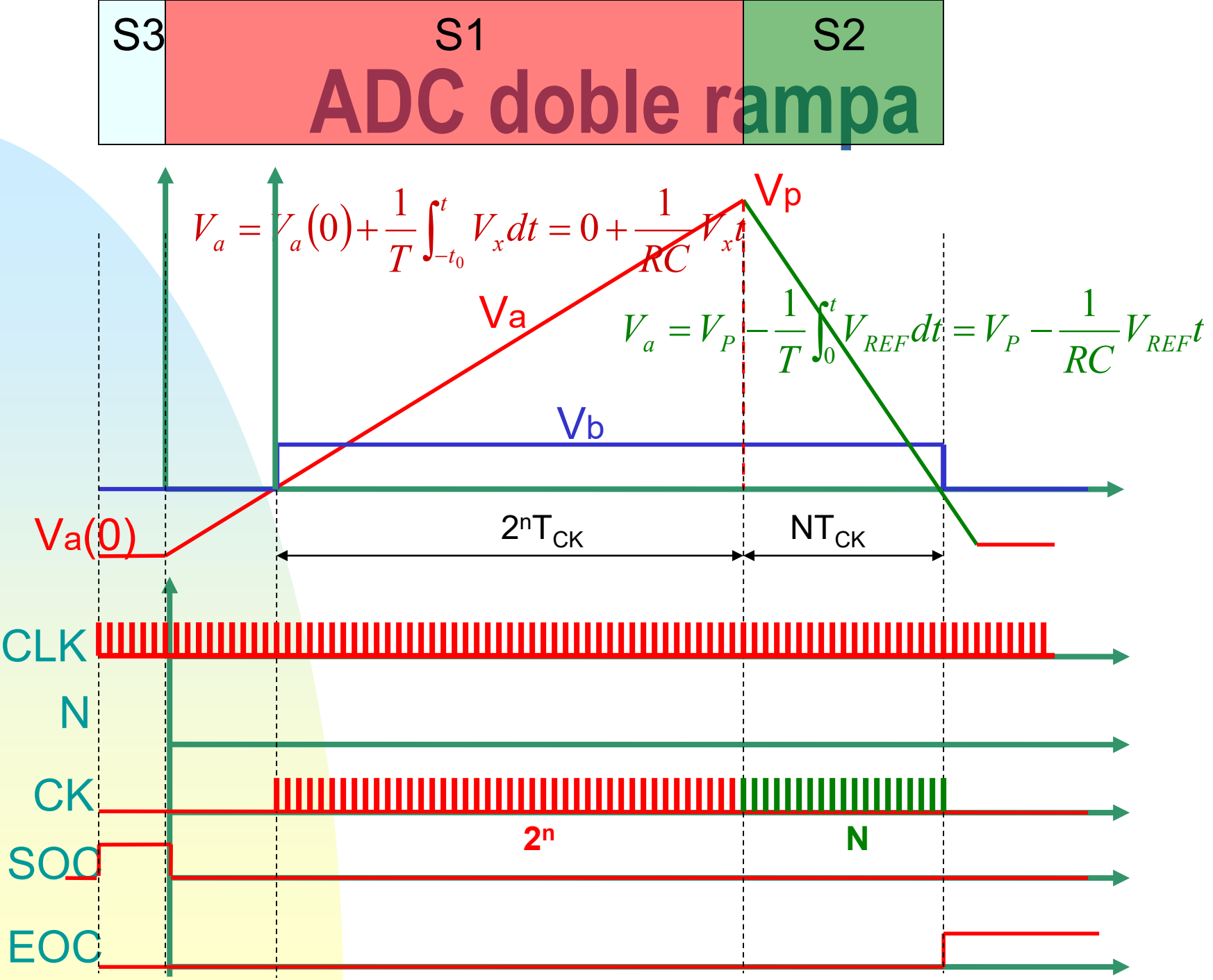
$$\frac{V_x}{V_{FS}} = \frac{N}{2^n}; \quad N = 2^n \frac{V_x}{V_{FS}}$$

ADC doble rampa



Simulación

ADC doble rampa



ADC doble rampa

$$V_a = V_a(0) + \frac{1}{T}\int_0^t V_x dt = 0 + \frac{1}{RC} V_x t$$

$$V_a = V_P - \frac{1}{T}\int_0^t V_{REF} dt = V_P - \frac{1}{RC} V_{REF} t$$

$$V_P = \frac{1}{RC} V_x 2^n T_{CK}$$

$$0 = V_P - \frac{1}{RC} V_{REF} N \cdot T_{CK}$$

$$\frac{1}{RC} V_X 2^n T_{CK} = \frac{1}{RC} V_{REF} N \cdot T_{CK}$$

$$V_X 2^n = V_{REF} N$$

$$N = \frac{V_X}{V_{REF}} 2^n$$

Diferencia de tiempos del orden de ms

ADC doble rampa (NMRR)

Si $v_x \neq \text{cte.}$ entonces $V_a = 0 + \frac{1}{T}\int_0^t v_x dt$

$$V_a = V_P - \frac{1}{T}\int_0^t V_{REF} dt = V_P - \frac{1}{T} V_{REF} t$$

$$V_P = \frac{1}{T}\int_0^{2^n T_{CK}} v_x dt$$

$$0 = V_P - \frac{1}{T} V_{REF} N \cdot T_{CK}$$

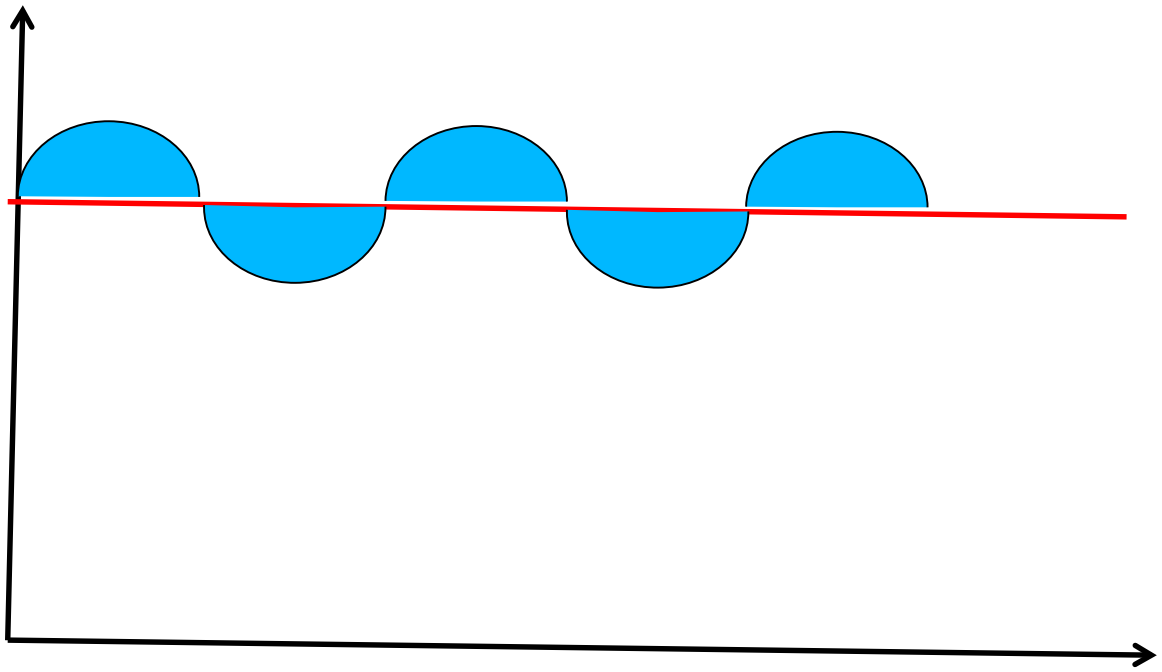
$$V_P = \frac{1}{T}\int_0^{2^n T_{CK}} v_x dt = \frac{1}{T} V_{REF} N \cdot T_{CK}$$

$$N = \frac{1}{V_{REF} \cdot T_{CK}}\int_0^{2^n T_{CK}} v_x dt$$

$$N = \frac{2^n}{V_{REF} \cdot 2^n T_{CK}}\int_0^{2^n T_{CK}} v_x dt = \frac{2^n}{V_{REF}} \frac{1}{2^n T_{CK}}\int_0^{2^n T_{CK}} v_x dt = \frac{2^n}{V_{REF}} \overline{V_x}$$

ADC doble rampa (NMRR)

$$N = \frac{2^n}{V_{REF}} \frac{1}{T_i} \int_0^{T_i} v_x dt = \frac{2^n}{V_{REF}} \frac{1}{T_i} \int_0^{T_i} \left[V_{DC} + V_N \cdot \sin(2\pi f t) \right] dt$$



Ejemplo de ADC doble rampa

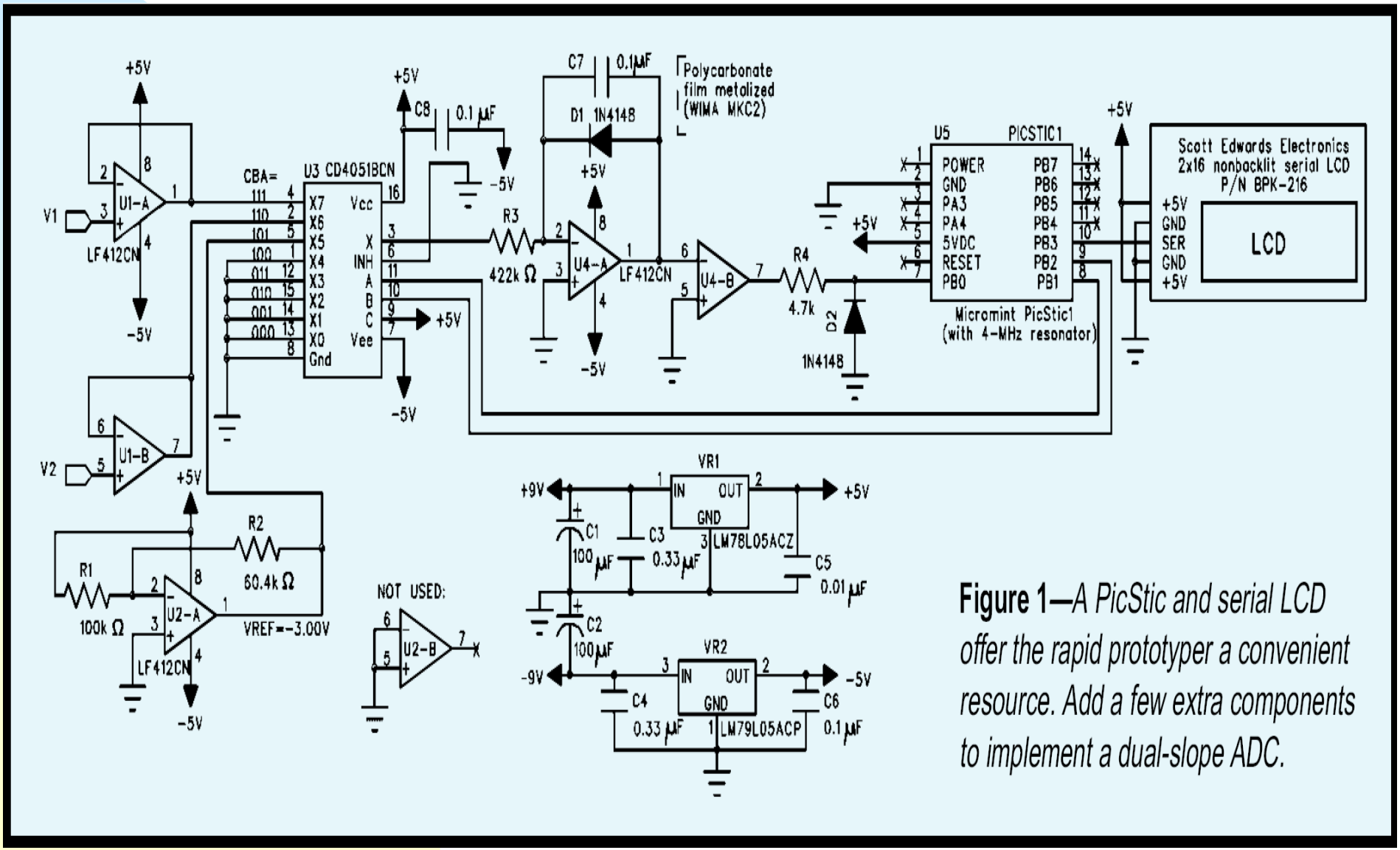


Figure 1—*A PicStic and serial LCD offer the rapid prototyper a convenient resource. Add a few extra components to implement a dual-slope ADC.*

ADC doble rampa

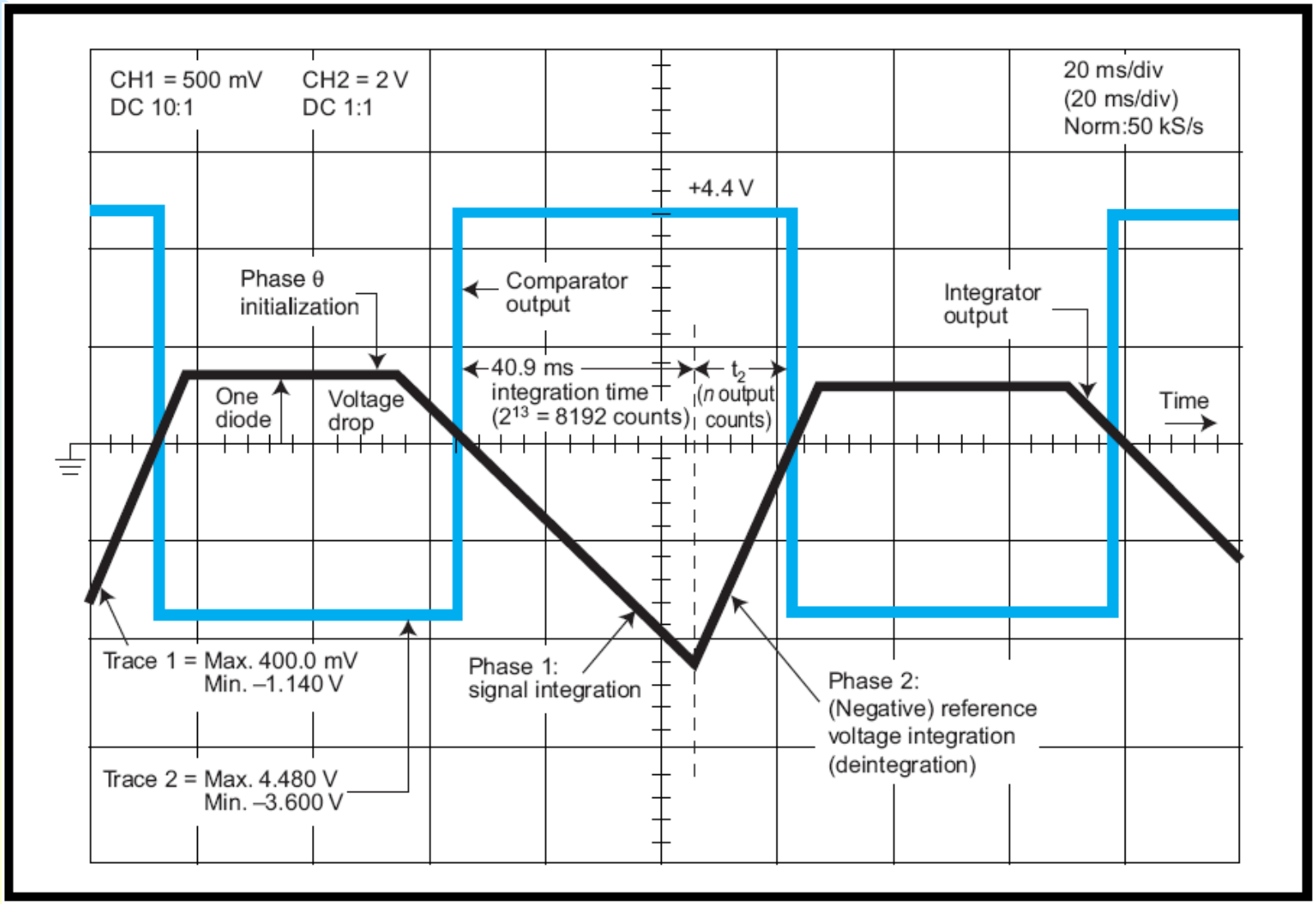


Figure 2—*Integration count begins when the falling voltage ramp passes through zero and ends after 8192 counts. The deintegration count then begins, ending only when the rising voltage ramp again passes through zero.*

ADC doble rampa

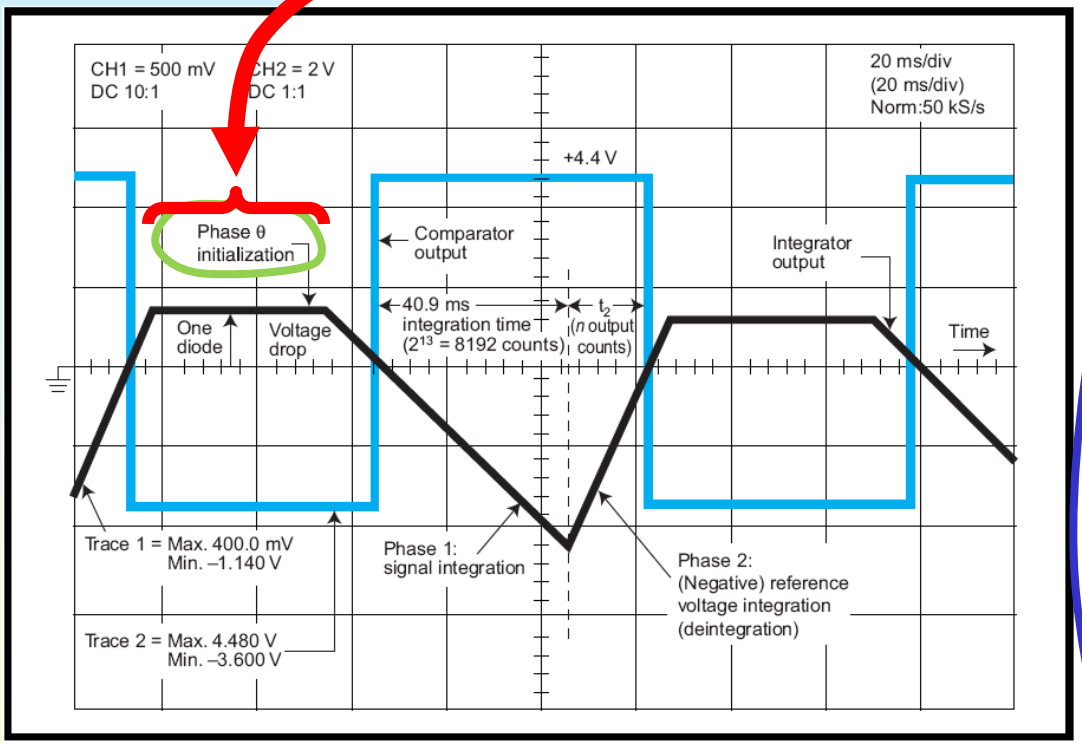
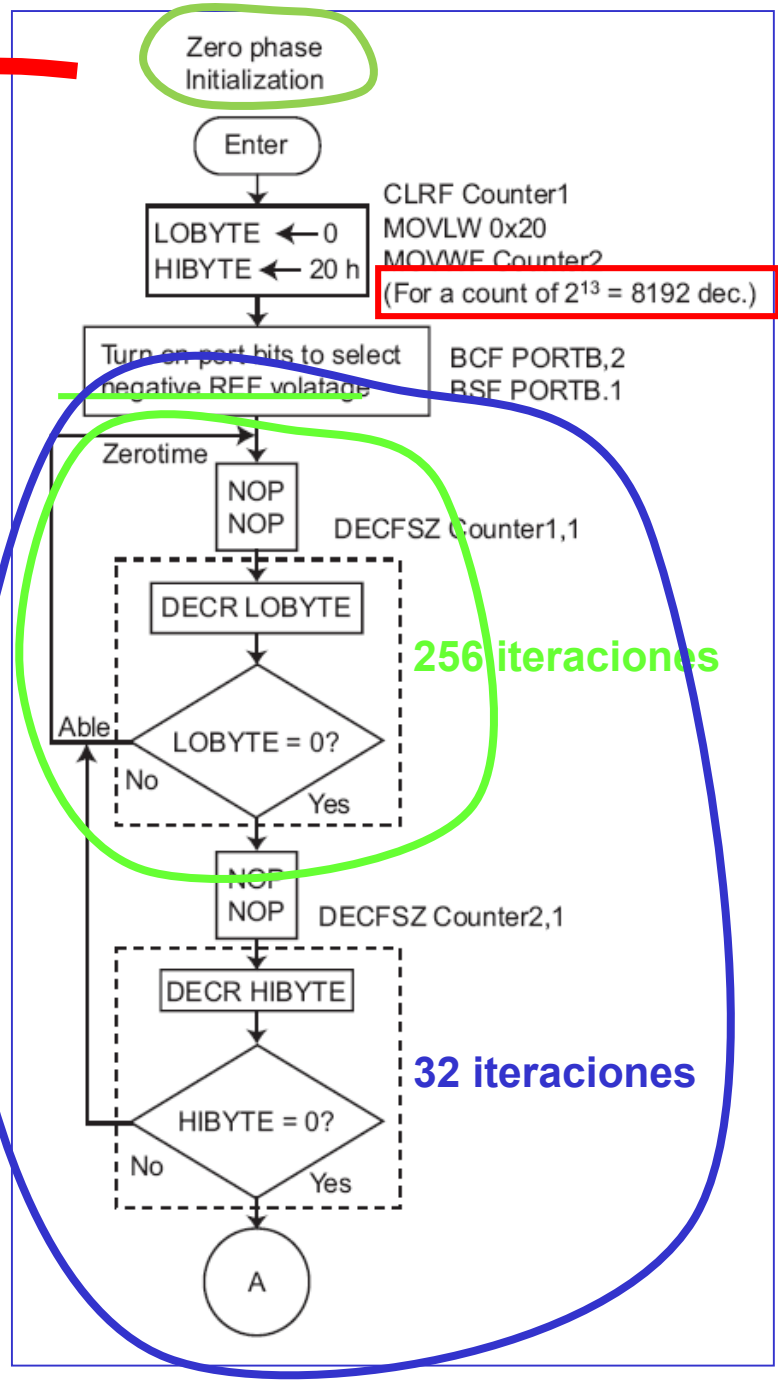


Figure 2—*Integration count begins when the falling voltage ramp passes through zero and ends after 8192 counts. The deintegration count then begins, ending only when the rising voltage ramp again passes through zero.*



ADC doble rampa

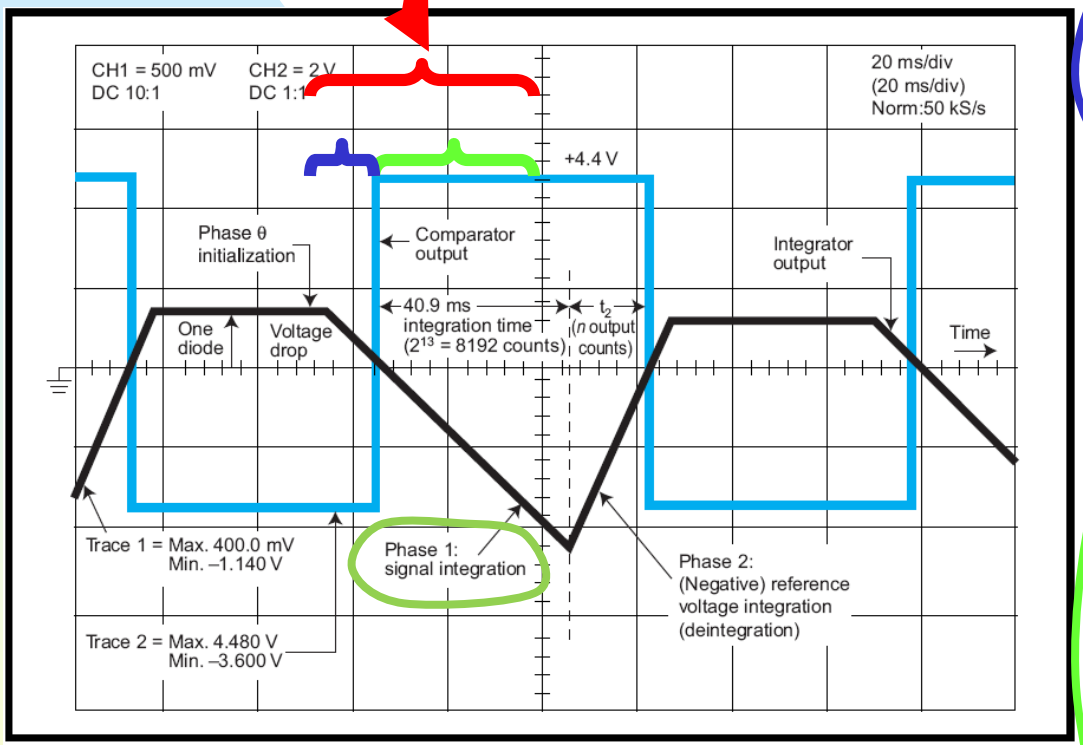
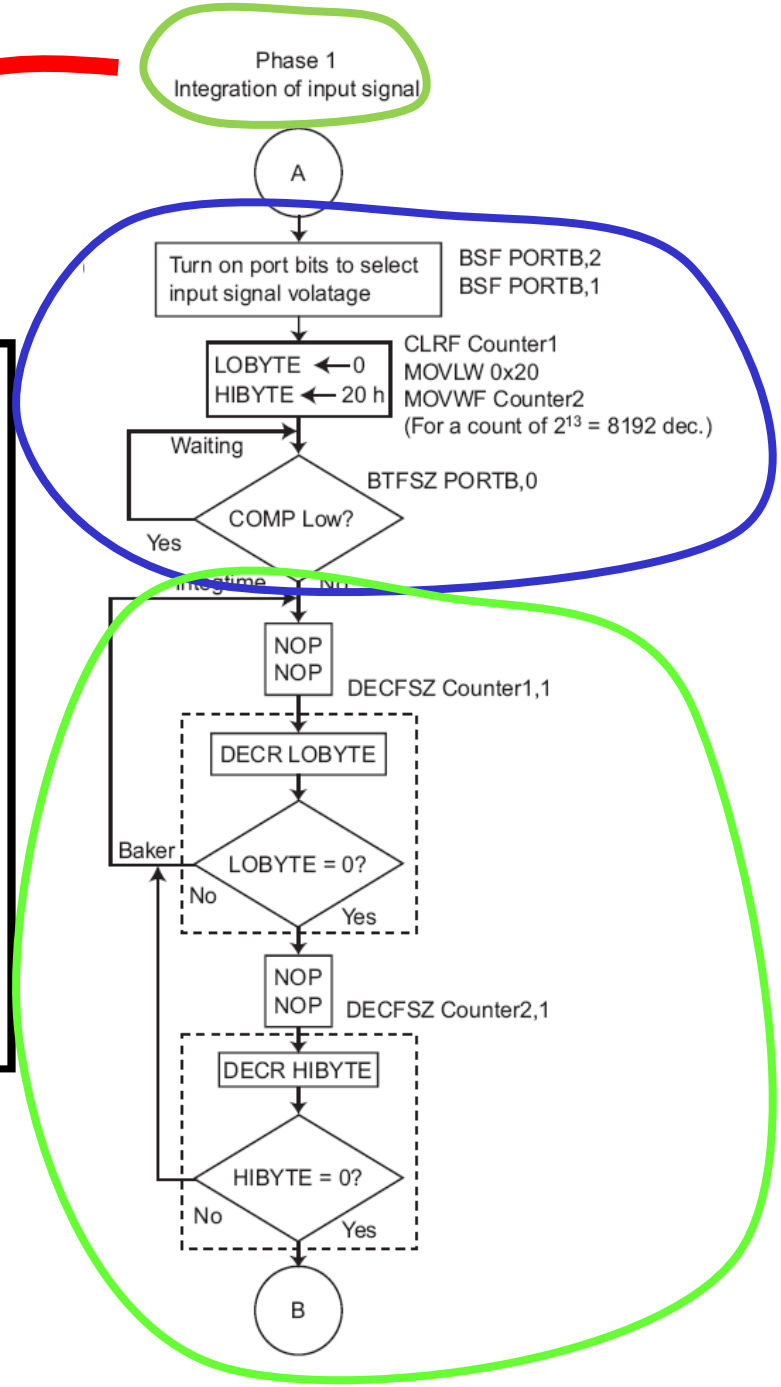


Figure 2—*Integration count begins when the falling voltage ramp passes through zero and ends after 8192 counts. The deintegration count then begins, ending only when the rising voltage ramp again passes through zero.*



ADC doble rampa

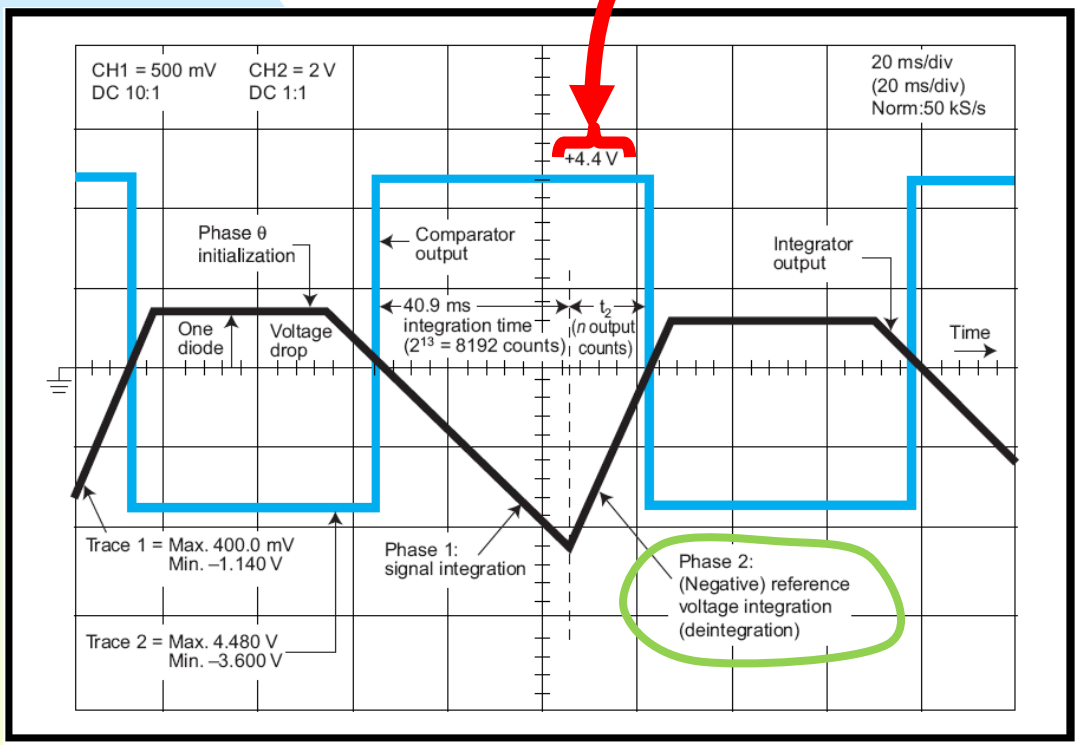
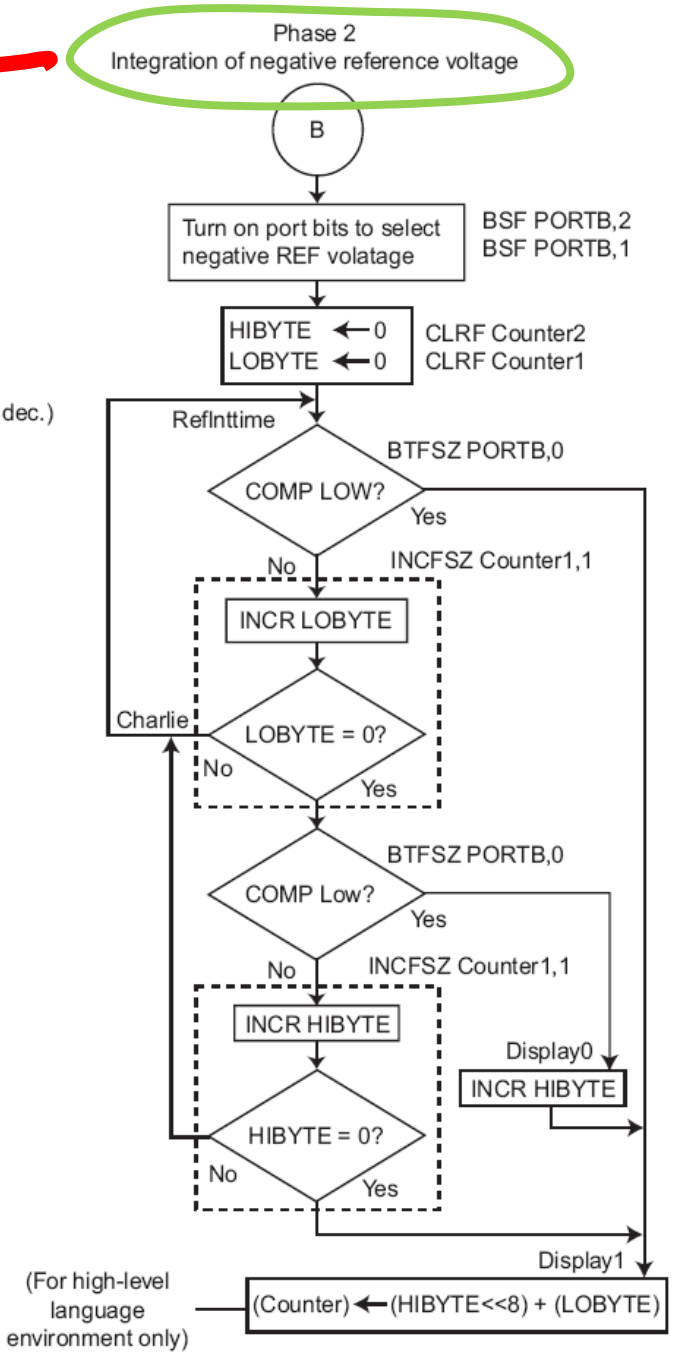
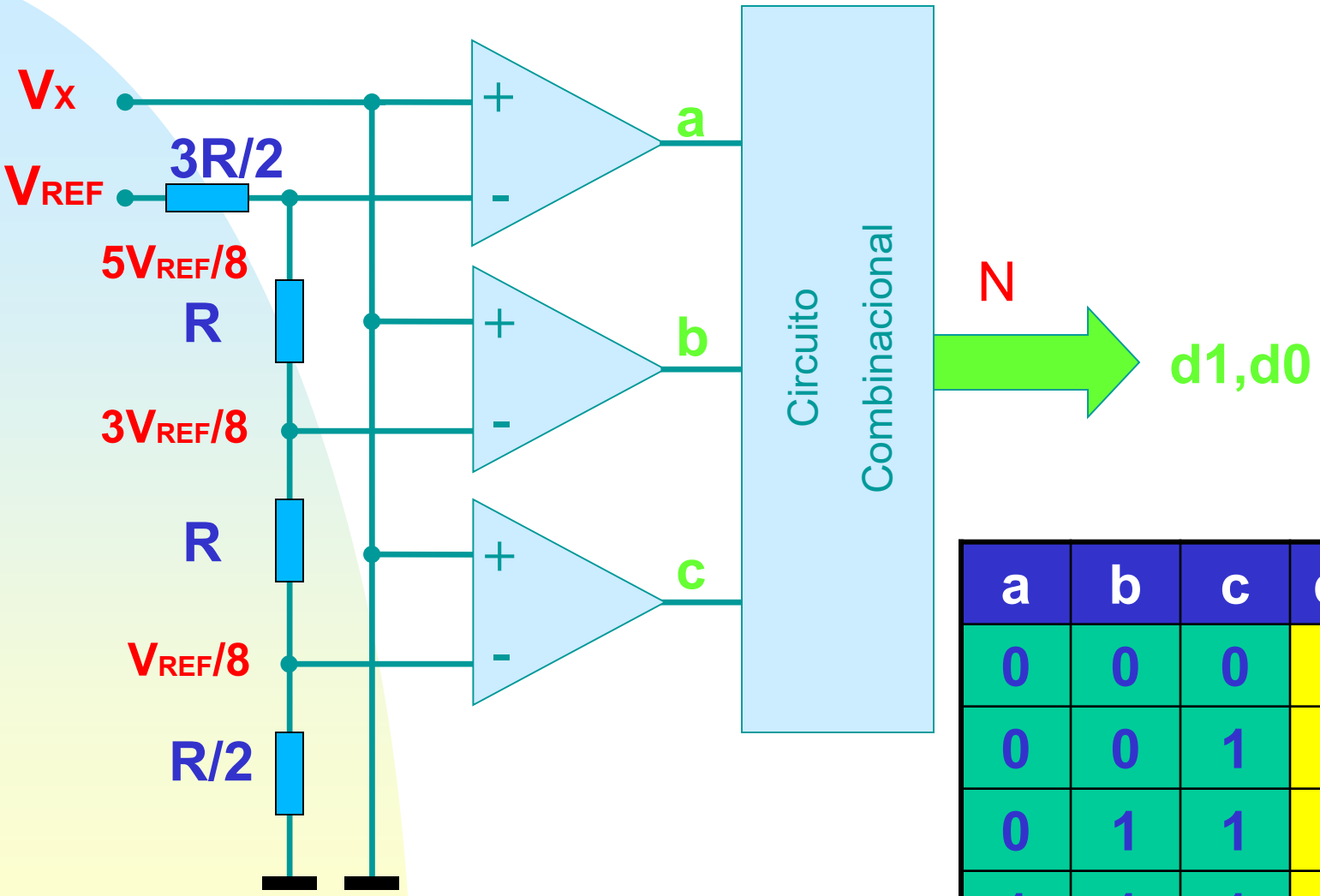


Figure 2—*Integration count begins when the falling voltage ramp passes through zero and ends after 8192 counts. The deintegration count then begins, ending only when the rising voltage ramp again passes through zero.*

I92 dec.)



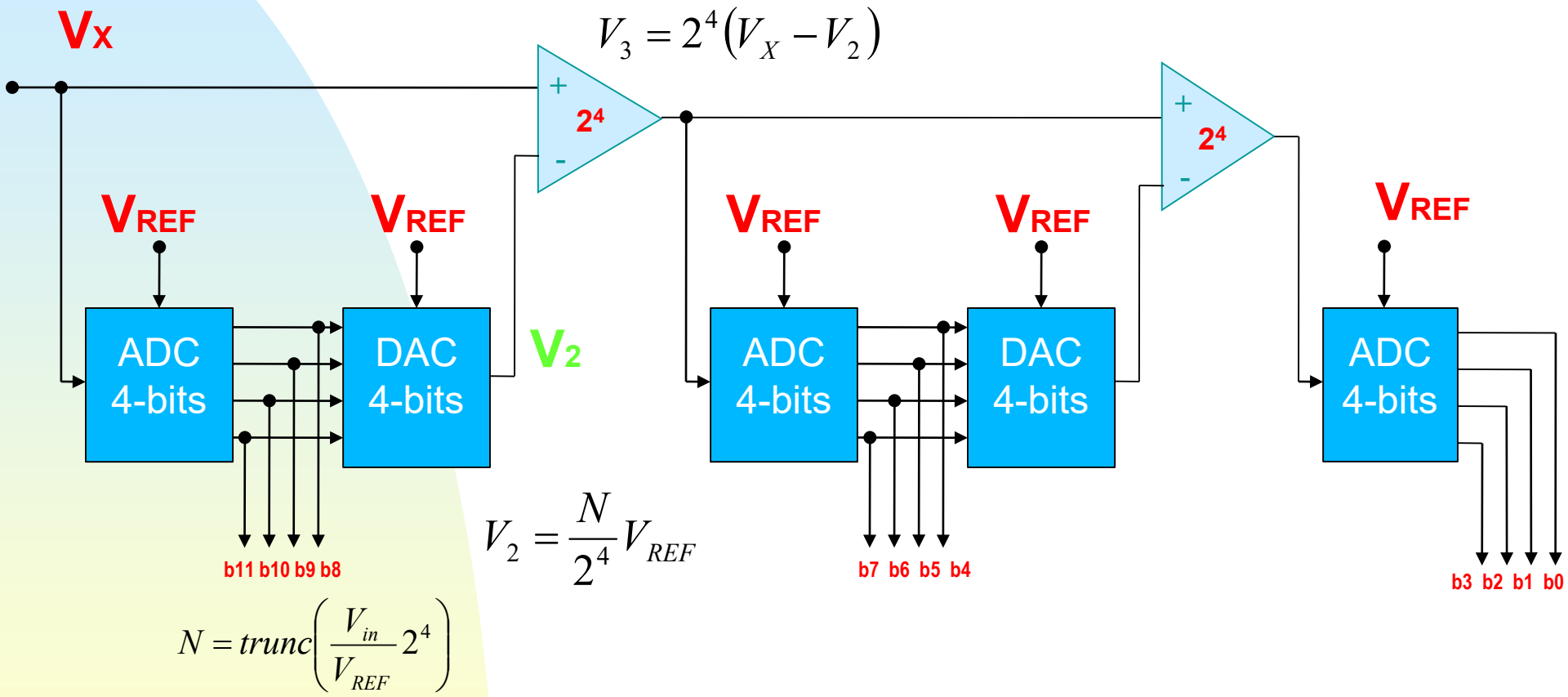
ADC Flash



a	b	c	d1	d0
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Simulación

ADC Half-Flash

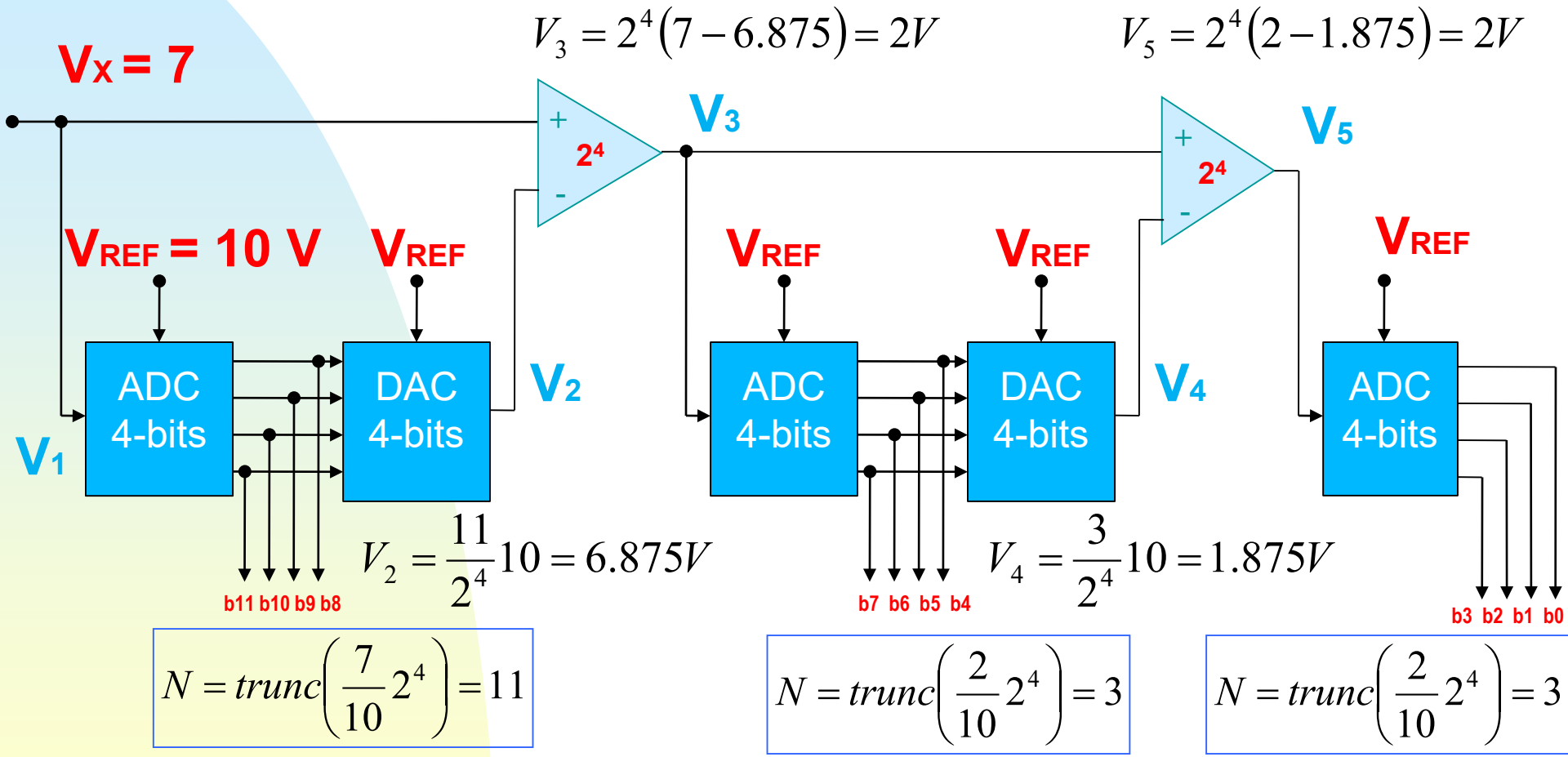


$$V_2 = \frac{N}{2^4} V_{REF}$$

$$N = trunc\left(\frac{V_{in}}{V_{REF}} 2^4\right)$$

Simulación

ADC Half-Flash



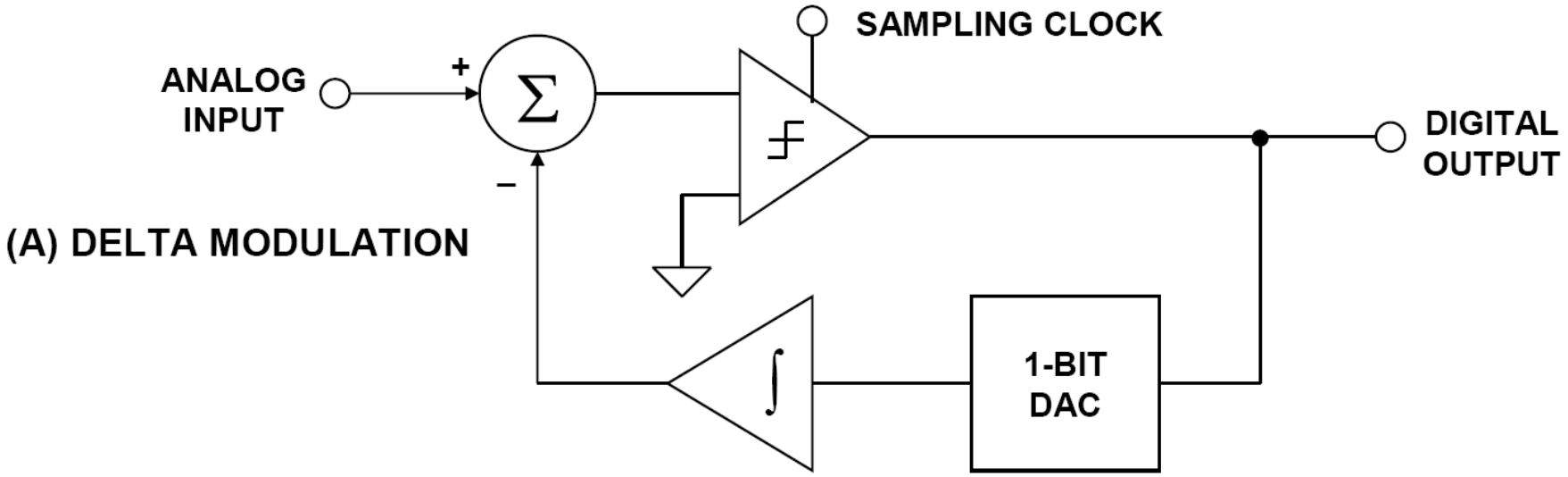
$$N = trunc\left(\frac{7}{10}2^{12}\right) = 2867 = B33_{16}$$

ADC Sigma-Delta

Modulación Delta:

- La señal analógica es cuantificada por un ADC de 1 bit (Comparador)
- La salida del comparador es nuevamente convertida a una señal analógica con un DAC de 1 bit
- y restada de la entrada, tras pasar por un integrador
- La forma de la señal analógica es transmitida así:
  - Un “1” indica que ha habido una variación positiva desde la última muestra
  - Un “0” indica que ha habido una variación negativa desde la última muestra

ADC Sigma-Delta



http://designtools.analog.com/dt/sdtutorial/sdtutorial.html

ADC Sigma-Delta

Figure 2: Quantization Using Delta Modulation

ADC Sigma-Delta

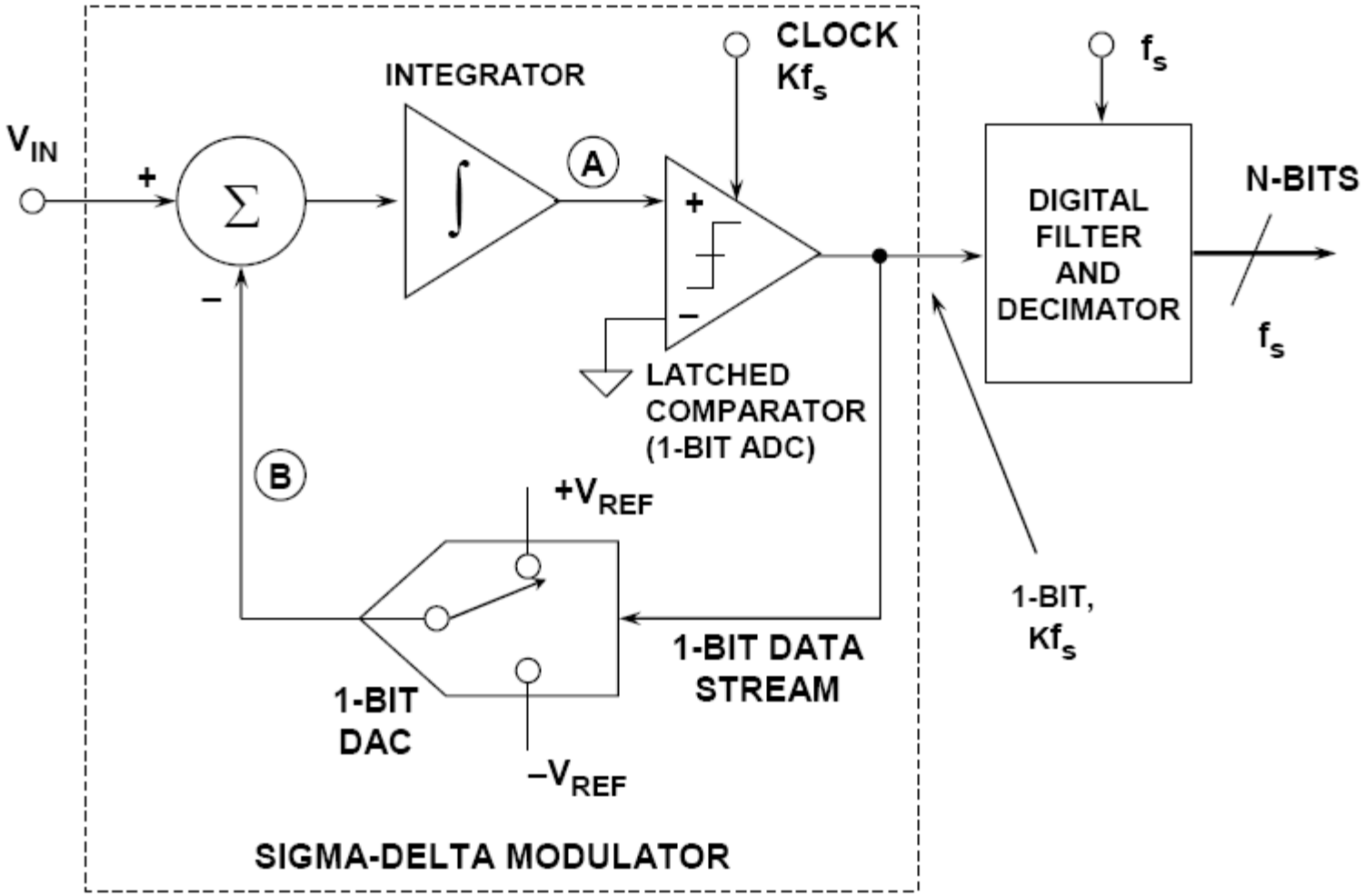


Figure 4: First-Order Sigma-Delta ADC

ADC Sigma-Delta

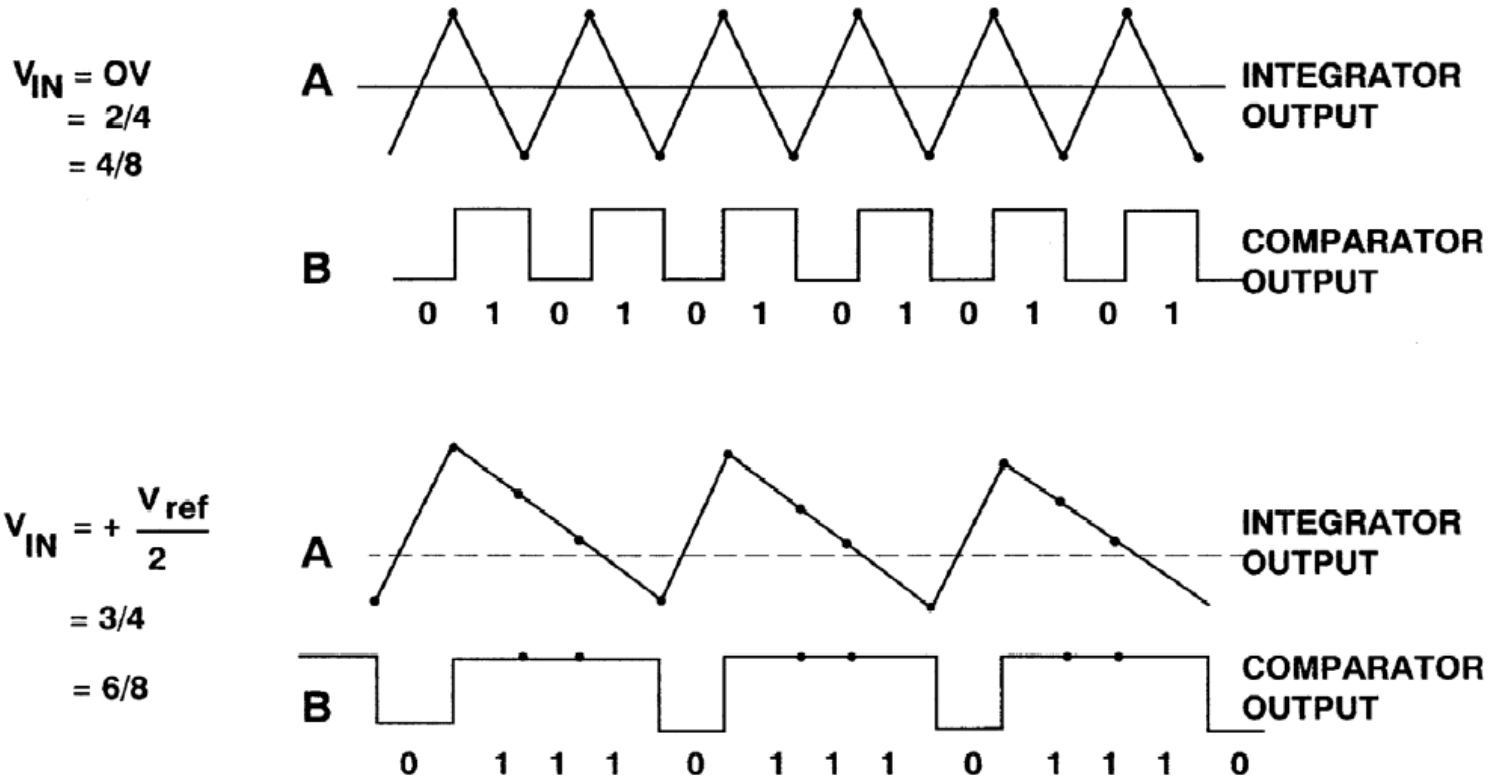


Figure 5: Sigma-Delta Modulator Waveforms

ADC Sigma-Delta

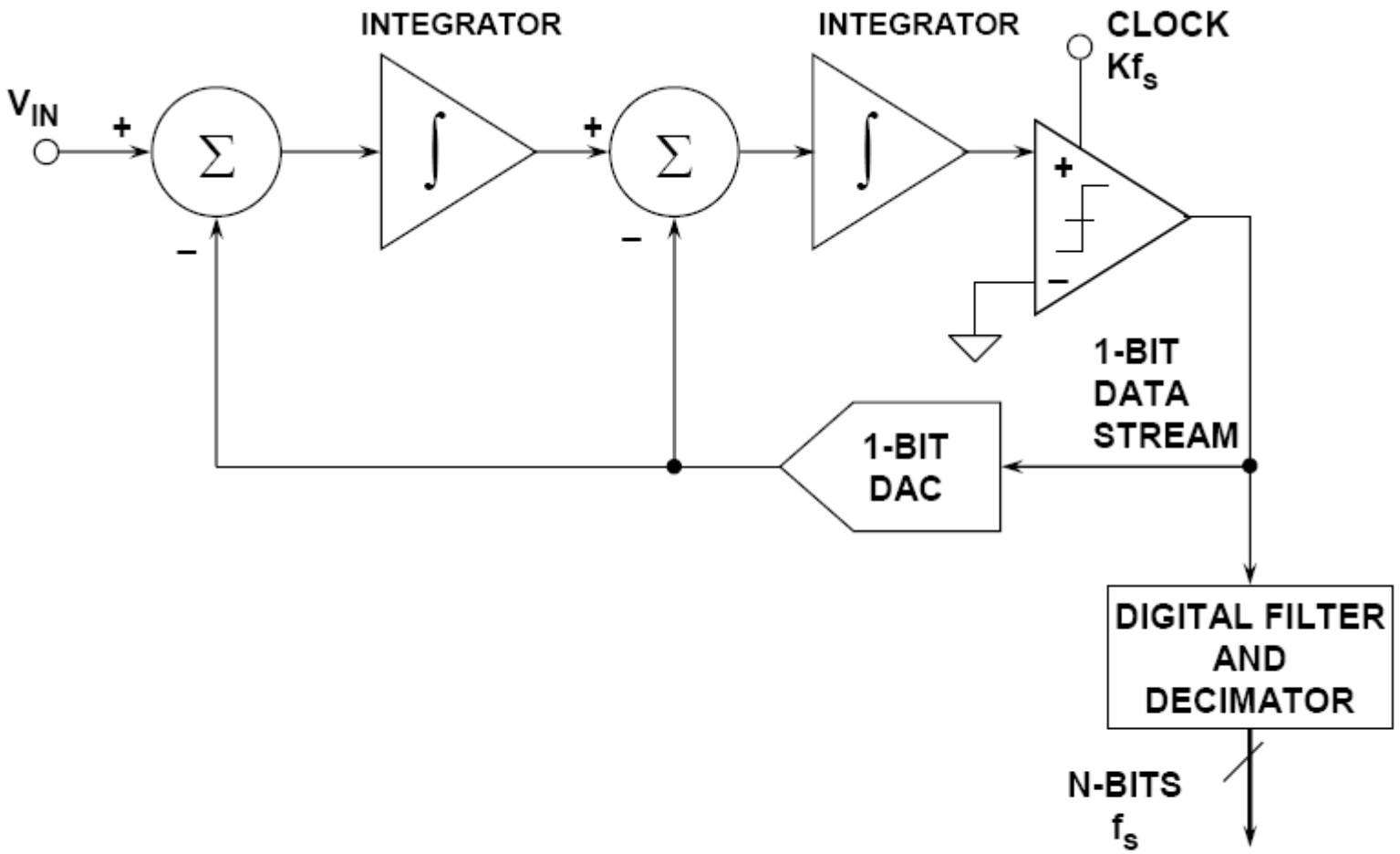


Figure 8: Second-Order Sigma-Delta ADC

ADC Comparación

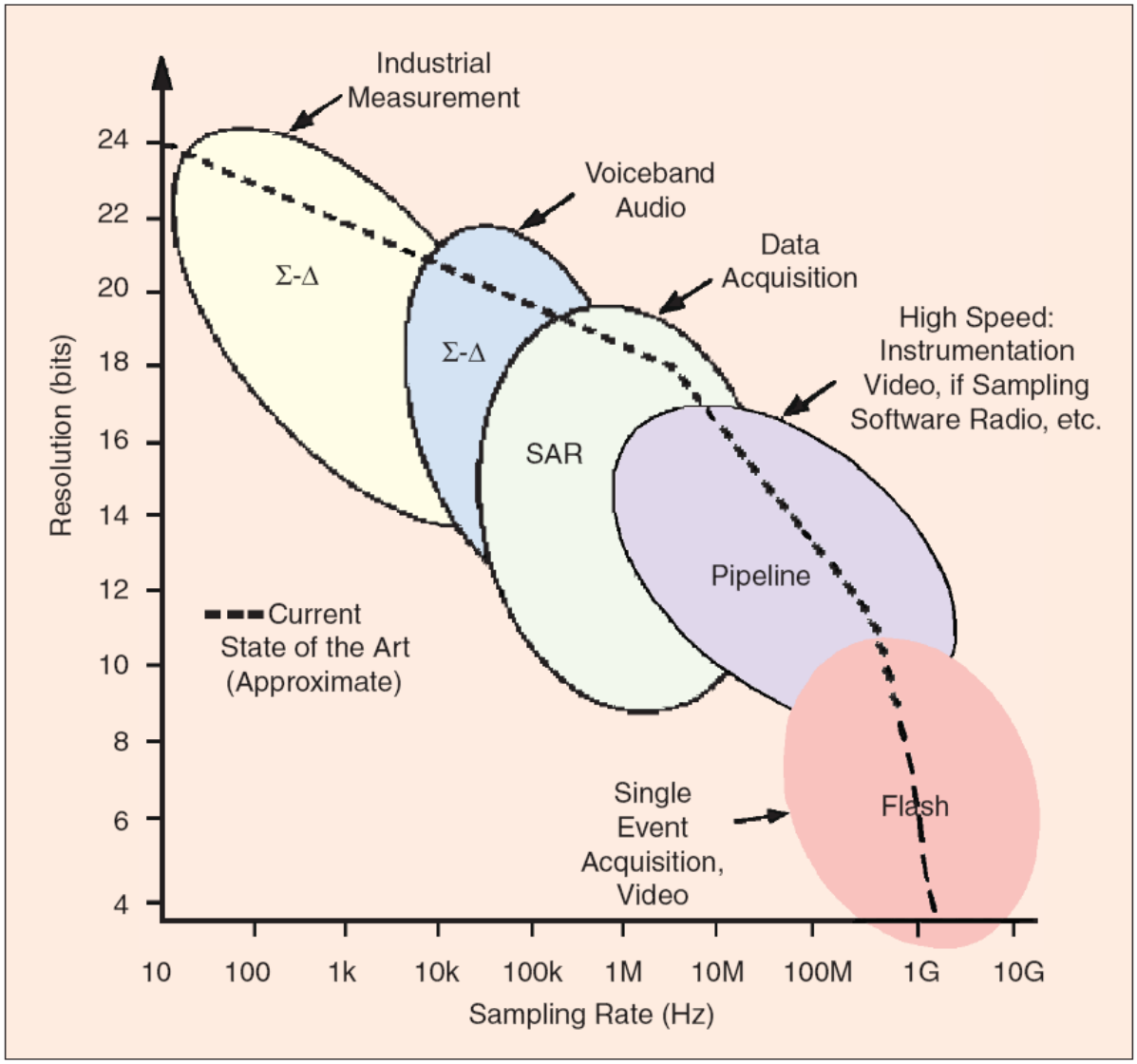
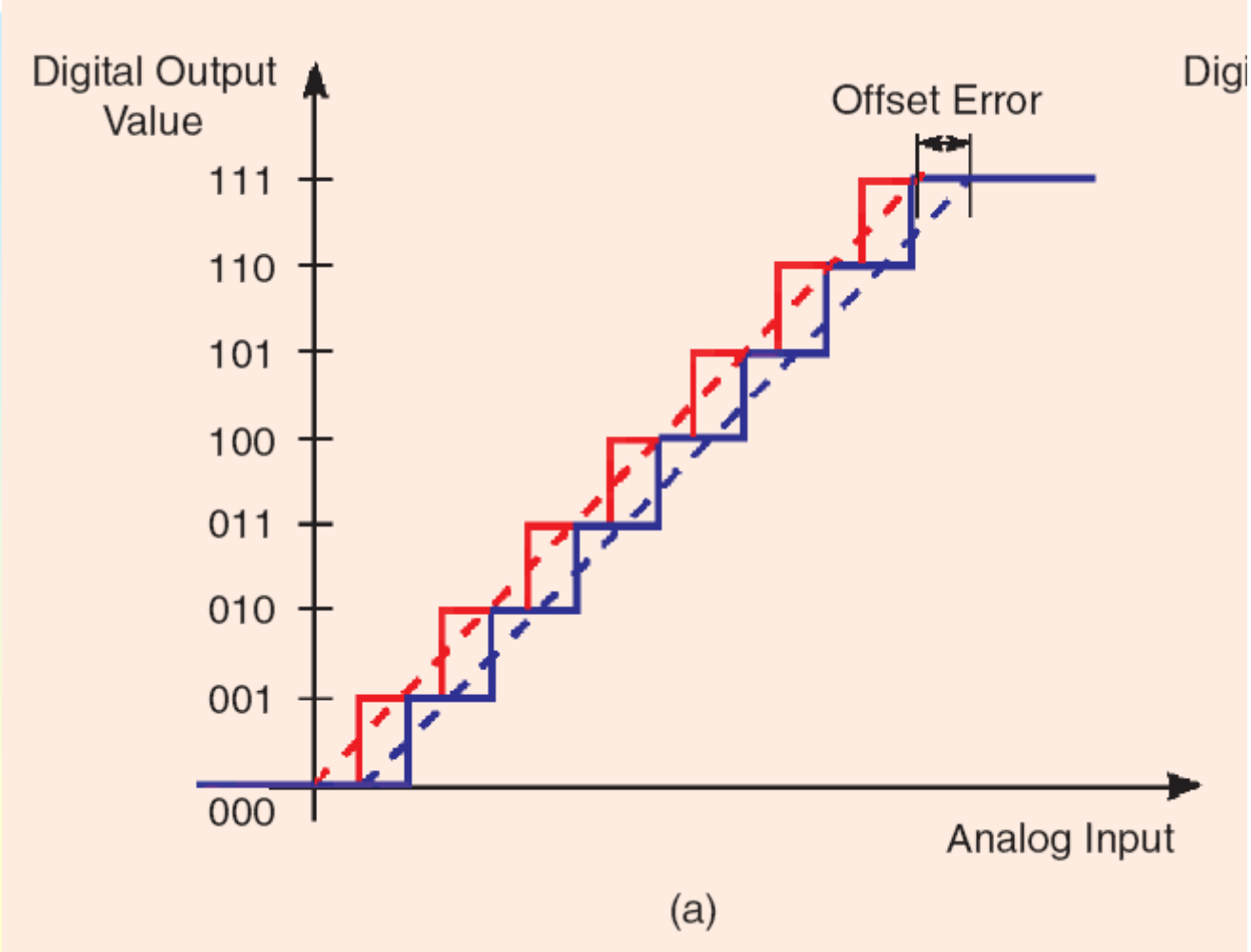
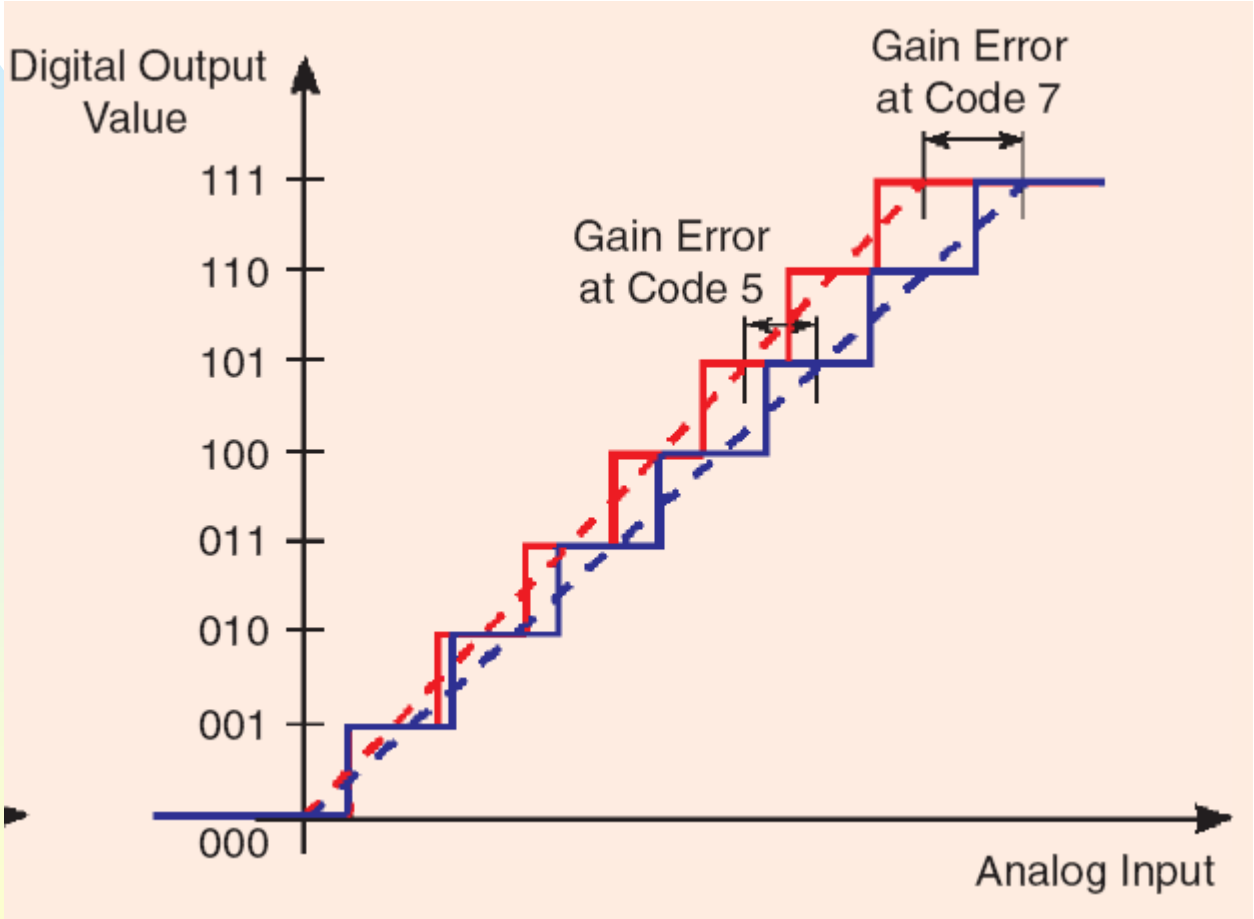


Fig. 1. ADC architectures, applications, resolution, and sampling rates.

ADC: Error de cero



ADC: Error de ganancia



ADC: Errores de cero y de ganancia

GAIN AND OFFSET ERRORS

Gain and offset errors represent the error contribution due to the displacement of the actual ADC characteristic from the reference one. The reference characteristic can be chosen according to several criteria. Most commonly used are the following:

- *Endpoint criterion:* the gain and offset errors are corrected such that the first and the last transition levels correspond exactly to the ideal ones.
- *Least square criterion:* the gain and offset errors are corrected such that the mean square deviation from the nominal reference transition levels are minimized.

ADC: Error No Linealidad Integral

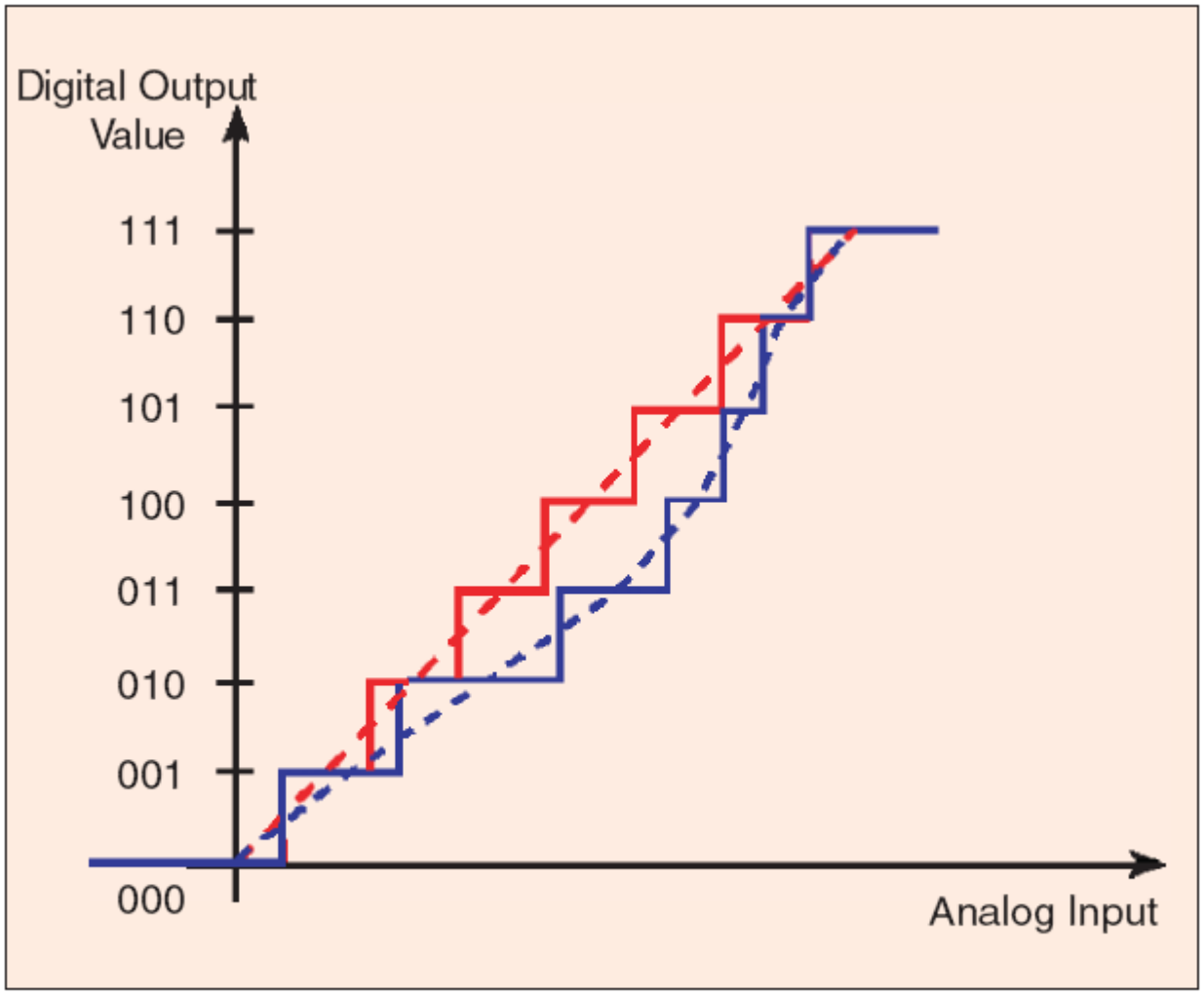


Fig. 10. INL causes the curve joining the middle point of each quantization step to not be a straight line.

ADC: Monotonicidad

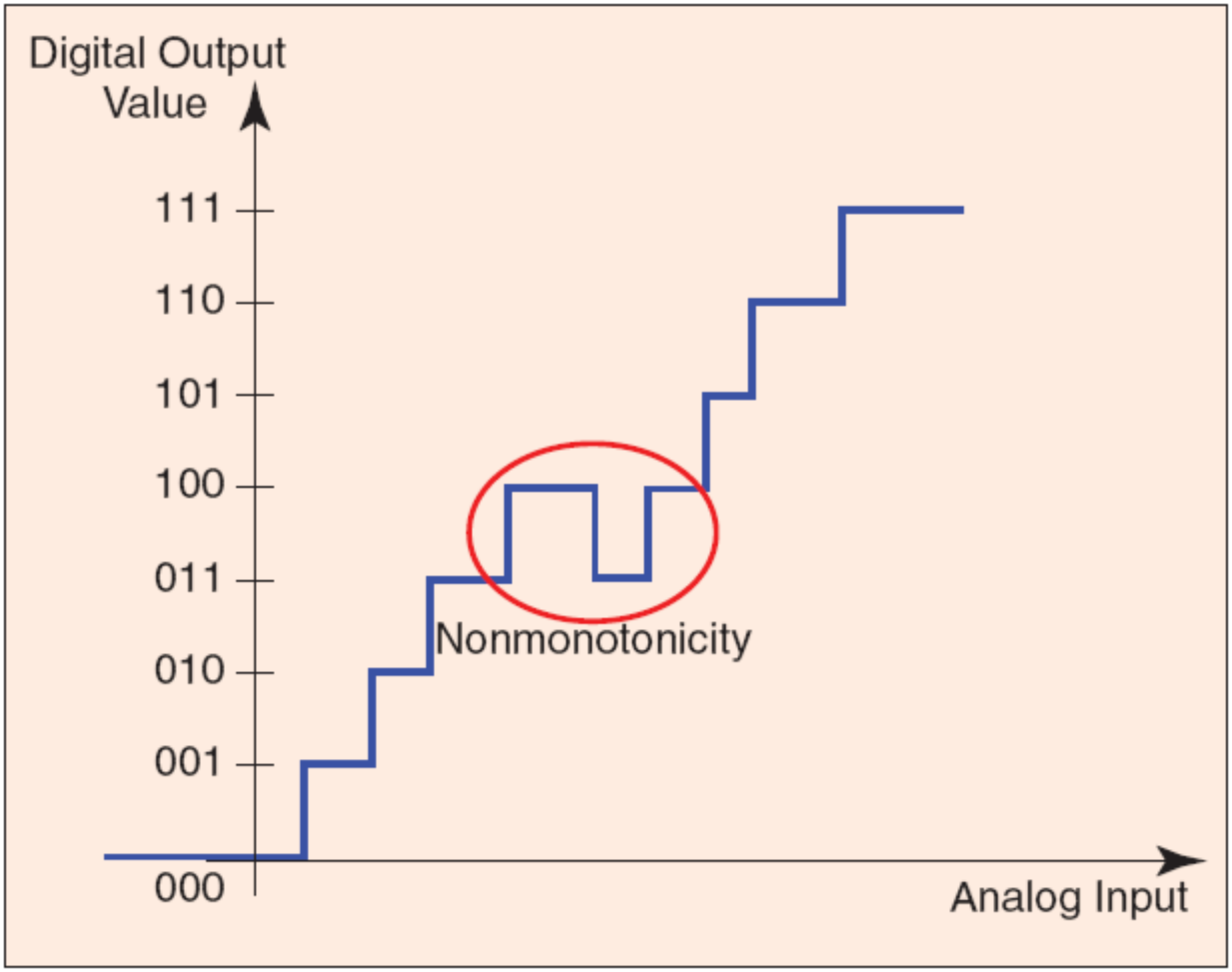


Fig. 11. The sample characteristic of a nonmonotonic ADC.

ADC: Monotonicidad

MONOTONICITY

An ADC is said to be monotonic if an increase or a decrease of the analog input signal correspond in every case to an increase or a decrease of the average digital output code (Figure 11). Such property is very relevant in applications where the stability is a key factor, such as in automatic control, where some variables are continuously tuned.

ADC: Histéresis

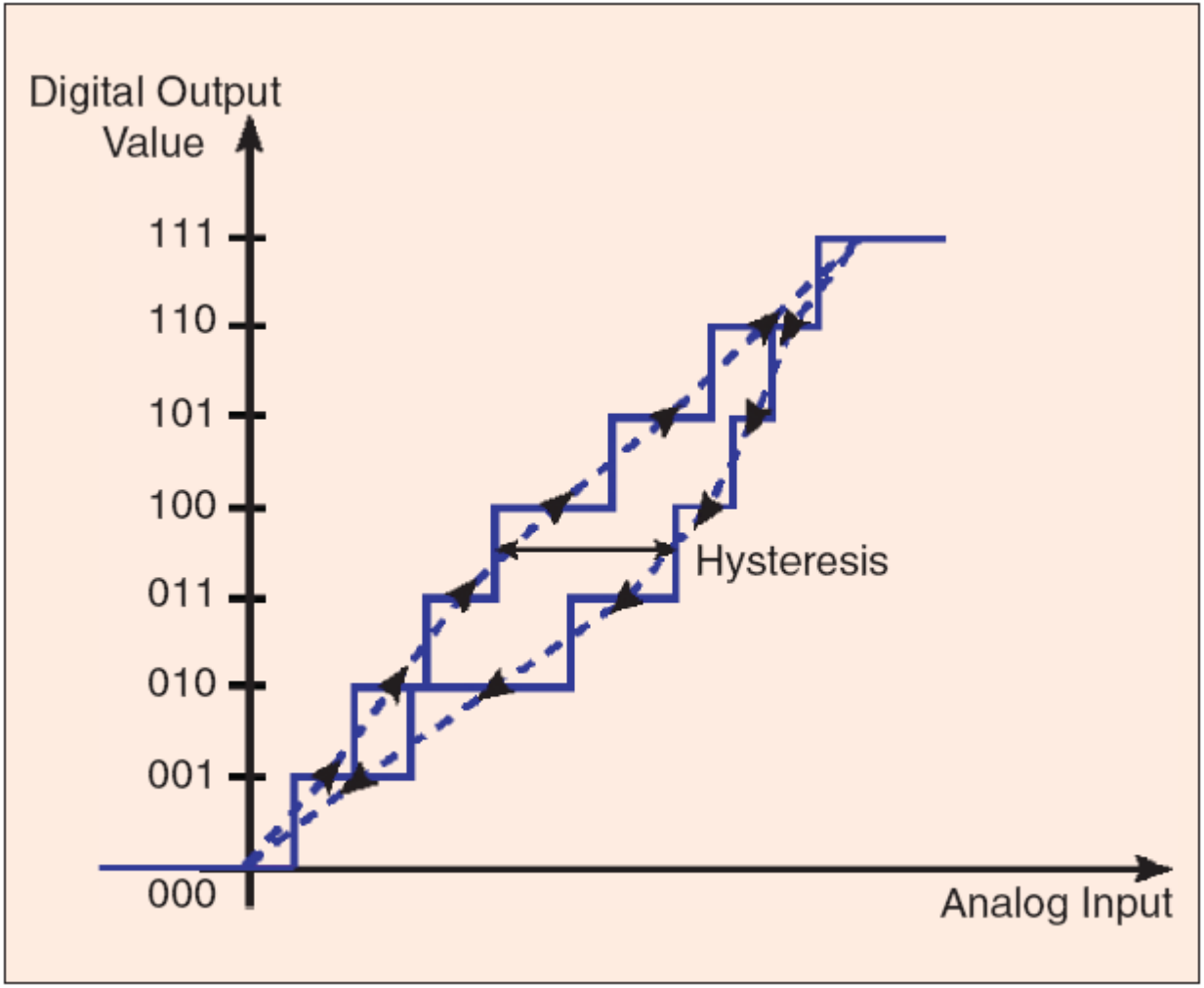


Fig. 12. The hysteresis shown on the characteristic.

ADC: Histéresis

HYSTERESIS

ADC characteristics often change when the slope of the input signal changes. In particular, two different curves can be observed when the input signal is increasing and decreasing. The hysteresis of an ADC is defined to be the maximum deviation of the transition levels (Figure 12). Hysteresis can be present at isolated code transitions. Hysteresis (and its complement, alternation) is evidence of feedback from previous ADC outputs into the input.

ADC: Errores y Especificaciones

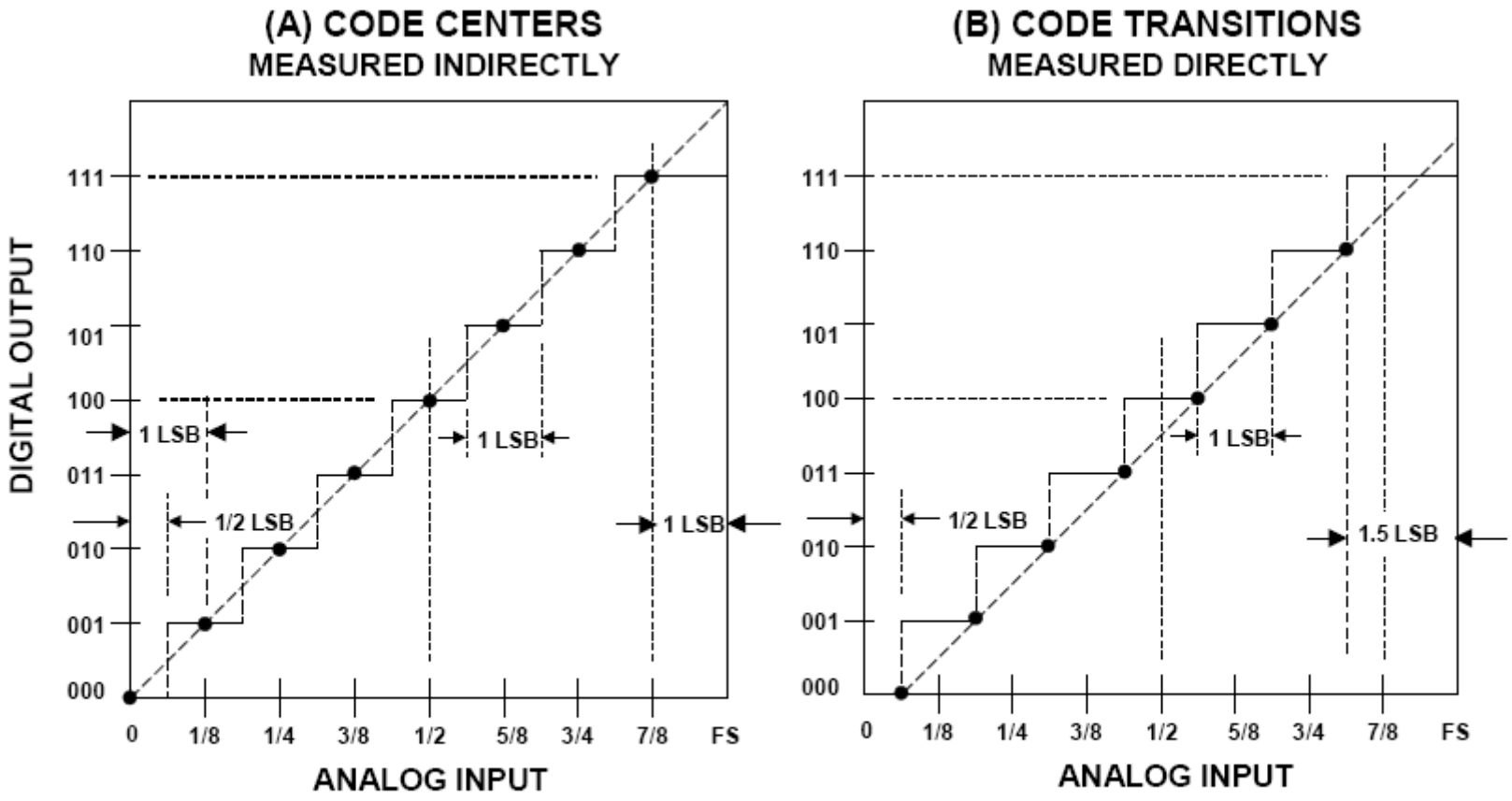


Figure 5.26: *Measuring ADC Code Transistions to Determine Code Centers*

ADC: Errores Offset y Ganancia

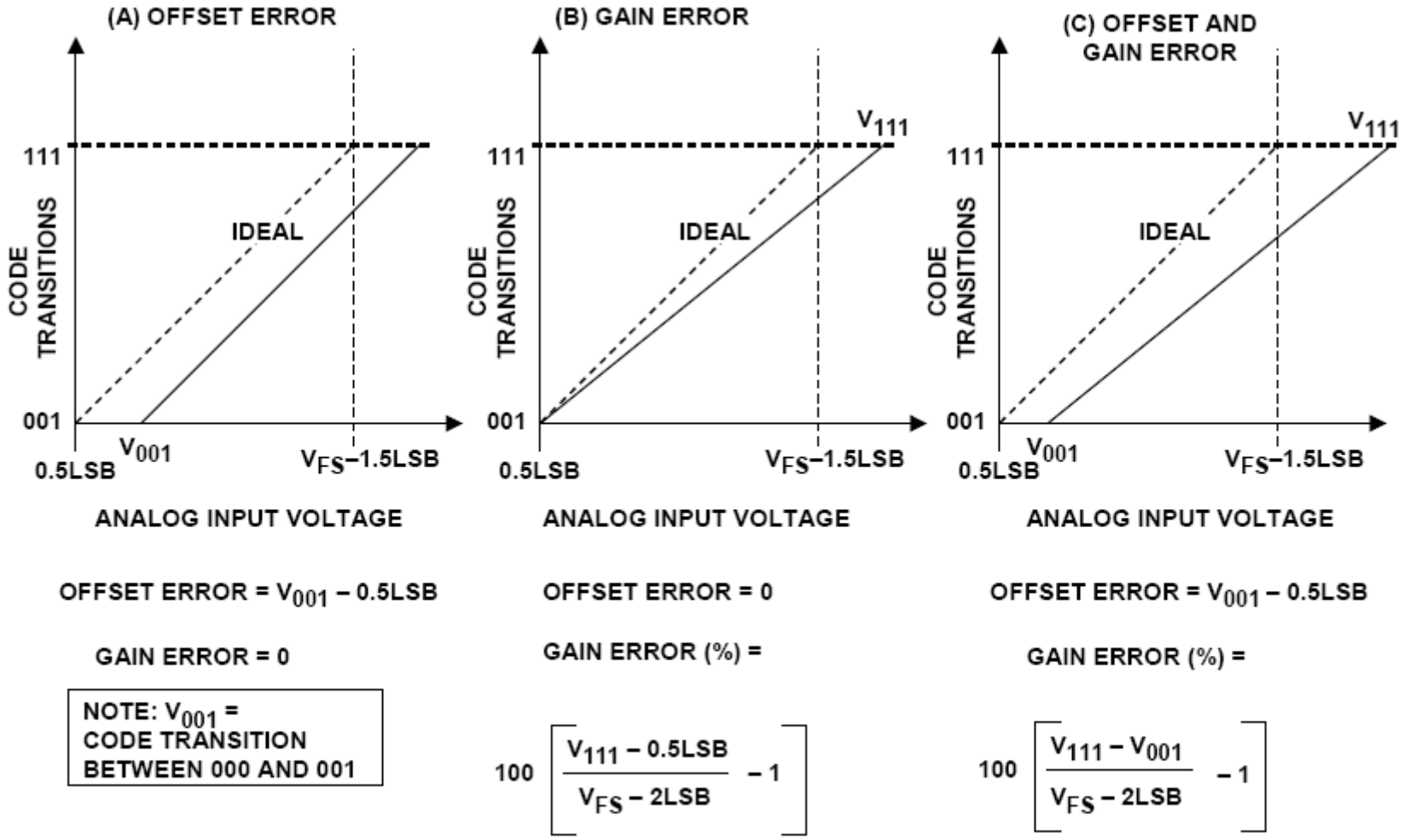
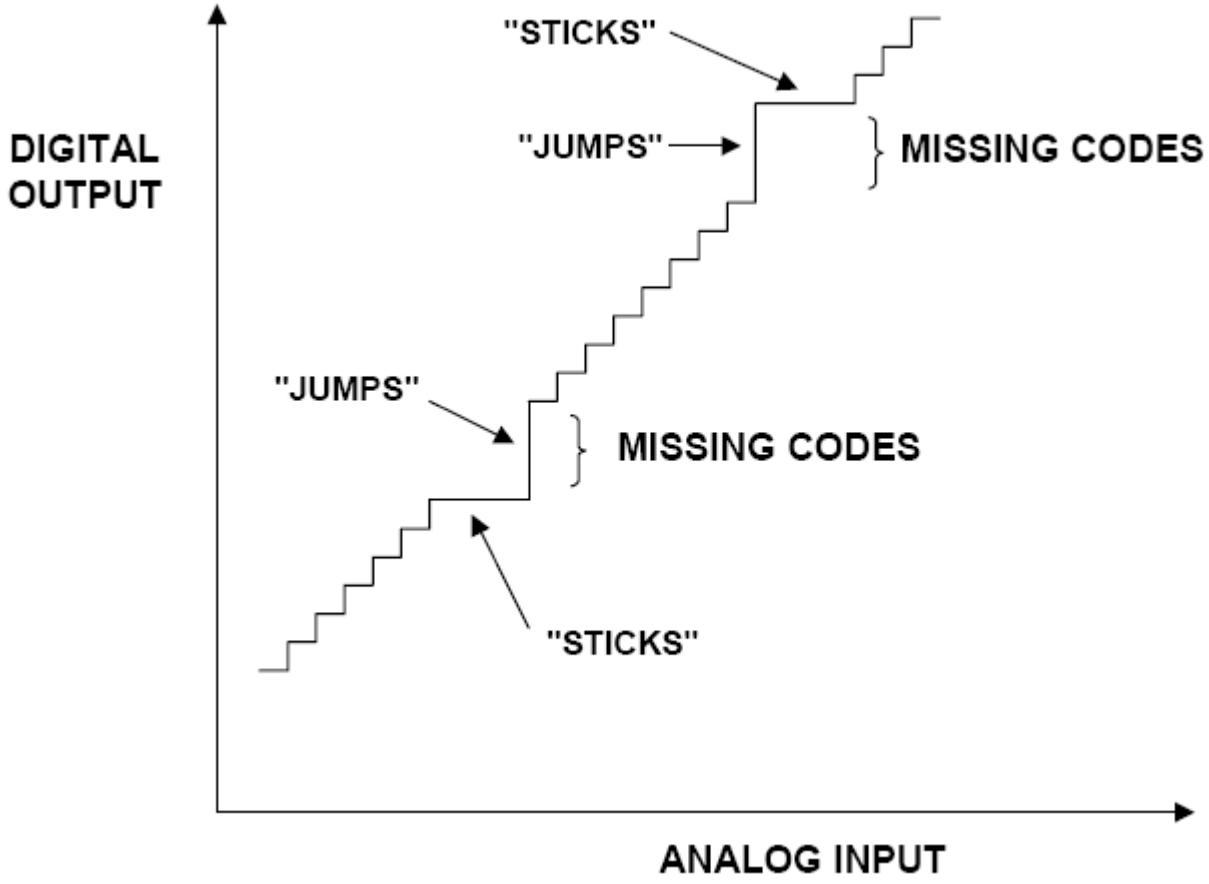


Figure 5.29: *Measuring ADC Offset and Gain Error*

ADC: Missing Codes



ADC: Selección

- http://www.analog.com/en/analog-to-digital-converters/ad-converters/products/index.html
- http://www.ti.com/lsds/ti/data-converters/analog-to-digital-converter-products.page
- http://www.microchip.com/pagehandler/en-us/products/analog/dataconverters/home.html